

DEVELOPMENT OF GALLIUM NITRIDE BASED BALLISTIC ELECTRON  
ACCELERATION NEGATIVE DIFFERENTIAL CONDUCTIVITY DIODES FOR  
TERAHERTZ POWER GENERATION: THERMAL AND ELECTRICAL  
MODELING, SIMULATION, PROCESSING AND CHARACTERIZATION

A Dissertation

Presented to the Faculty of the Graduate School  
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by

Barbaros Aslan

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The portion of the electromagnetic spectrum that lacks any viable devices is that in the region near one terahertz. Neither lasers nor electronic devices have reached this important frequency range to date. Compact, continuous wave (CW) and room temperature devices that will generate much greater than one milliwatts of power are being sought for medical, security and many other important applications. Today, the only viable solid state device seems to be the quantum cascade laser which has only recently been improved to work around room temperature, and is capable of only a couple of hundred nanowatts THz energy output.

This dissertation presents a comprehensive treatment of the processing, modeling, electrical/thermal simulations, and characterization of a revolutionary device concept - the ballistic electron acceleration negative differential conductivity (BEAN) diode - and its potential for electronic THz power generation. Wurtzite GaN has been the material of choice for two reasons: (i) its strong inflection point (to harness the negative effective mass quantum states) and (ii) its capability of withstanding a few MV/cm electric fields due to its 3.4 eV band gap. Two different device concepts

based on electron acceleration in GaN were investigated as part of this research effort. These are ballistic negative effective mass (vertical) diodes and Quasi-ballistic (horizontal) diodes.

In the first half of this dissertation, the quantum theoretic foundations of the negative effective mass diode will be explained and subsequent experimental results will be discussed. The details of the process development for different structures will follow. In the second half, similarly, both the theoretical foundations and experimental results on the quasi-ballistic horizontal device will be presented. Results on large-signal circuit and transient thermal simulations will be presented with discussions. The proposed diode operation in this section is in accumulation-layer transit-time mode and conversion efficiencies up to ~3.4 % at ~1.5 THz are shown to be possible. This is followed by a detailed account of the process development on this particular device. We conclude the dissertation with a chapter devoted to the ohmic contact studies on  $n^{++}$  doped GaN ( $1 \times 10^{20} \text{ cm}^{-3}$ ). The need for such studies arose from destructive joule heating at poor contacts and the intolerable voltage that drops across them.

## BIOGRAPHICAL SKETCH

Barbaros Aslan was born in Istanbul, Turkey, on April 27, 1978. He completed his early education in Istanbul, Turkey. In 1996, he graduated from Ozel Ata High School. He then enrolled as an engineering student at Istanbul University in 1997. After graduating with a BS degree in electrical engineering in 2001, he began his PhD studies at Syracuse University, Syracuse, New York. Upon completing his required coursework and passing qualification exams, he began his research with emphasis on computational electromagnetics. During his studies there, he did summer research for the company Anaren Microwave and a full academic year funded research for Herley Industries (a defense contractor).

Later on, his research interest shifted towards semiconductor devices, particularly III-V's. Upon his application, he got admission to Cornell University in 2005 to join Professor Lester Eastman's research group at Cornell University as a PhD candidate. As a result of this, he changed his degree and obtained an MS degree from Syracuse University. At Cornell, he undertook the research and development of GaN based ballistic electron acceleration negative differential conductivity diodes. His PhD research efforts at Cornell focused entirely on the design, simulation (electrical and thermal), fabrication and characterization of these two terminal devices.

*To my wife Asma and my family*

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# CHAPTER 1

## Introduction

### 1.1 Current State of THz Semiconductor Device Research

A promising optical source of THz emerged in the last years with the quantum cascade laser. Quantum cascade lasers (QCL) emit in the mid to far-infrared portion of the electromagnetic spectrum and were first demonstrated at Bell Laboratories in 1994 [1]. Output powers of a few miliwatts at several THz have been demonstrated [2] showing that THz QCLs are a probable source for the future. However; such structures are still very difficult to elaborate and an important drawback is the operating temperature which is below that of liquid nitrogen. This is the case mainly due to the difficulty encountered in reducing the interactions with phonons. Problems like poor coupling of its optical modes to free space and material related issues also remained in the way. In 2008, a group of engineers and applied physicists at Harvard University have demonstrated an improved version of QCL approach which outputs only several hundred nanowatts, this time *at room temperature*. They attached a 2 mm-diameter Silicon hyper-hemispherical lens to the facet of the device to collimate the 5 THz terahertz output signal [3].

Another possibility for a solid state THz source was recognized with the discovery of the THz emission in InGaAs and GaN HEMTs which was recently reported by Knap et al. [4] and Deng et al. [5]. Ryzhii and Shur et al [6] proposed an explanation to these oscillations through coupled spatio-temporal variations of the electron density and the electric field (electron plasma oscillations). They developed a device model which is

designed to excite these oscillations. However such a device has not yet been reported to work as an efficient source of THz radiation.

In conclusion, up to date, these two have been the only promising solid state approaches to generate reasonable THz power levels. Therefore, a compact source of electronic THz signal which does not need elaborate liquid nitrogen cooling and capable of emitting in the milliwatts range is still the Holy Grail in THz device research. The revolutionary device idea that will be explored in this dissertation is based on unique GaN ballistic transport properties and is the third important candidate for the realization of such a source.

## **1.2 Ballistic Transport Properties of Wurtzite GaN**

GaN has been the material of choice in this research for two main reasons. First one is the fact that it has a strong band nonparabolicity in the  $\Gamma$  valley up to 2.7 eV energy. This is an inflection point approximately 1 eV above the conduction band minimum. If one can efficiently accelerate the electrons beyond that energy, the electrons will be in negative effective mass quantum states and therefore they will *decelerate* under the influence of the same electric field which accelerated them. This is quite counter intuitive from a Newtonian mechanics perspective of motion; however, it is possible in the Wurtzite GaN crystal. It will manifest itself only if one can put such a high electric field across a short channel of GaN in the order of a mean free path ( $\sim 20\text{-}30$  nm). This brings us to the second important key feature of the GaN band structure: It's 3.4 eV band gap. It allows the crystal to withstand very high electric fields (in the order of a few MV/cm) without break down. This is important since the availability of the negative mass states would be useless unless you can put the electrons there without causing avalanche breakdown. The 3.4 eV band gap therefore makes GaN a possible

candidate for harnessing this peculiar quantum mechanical phenomena in order to create oscillations in the THz range.

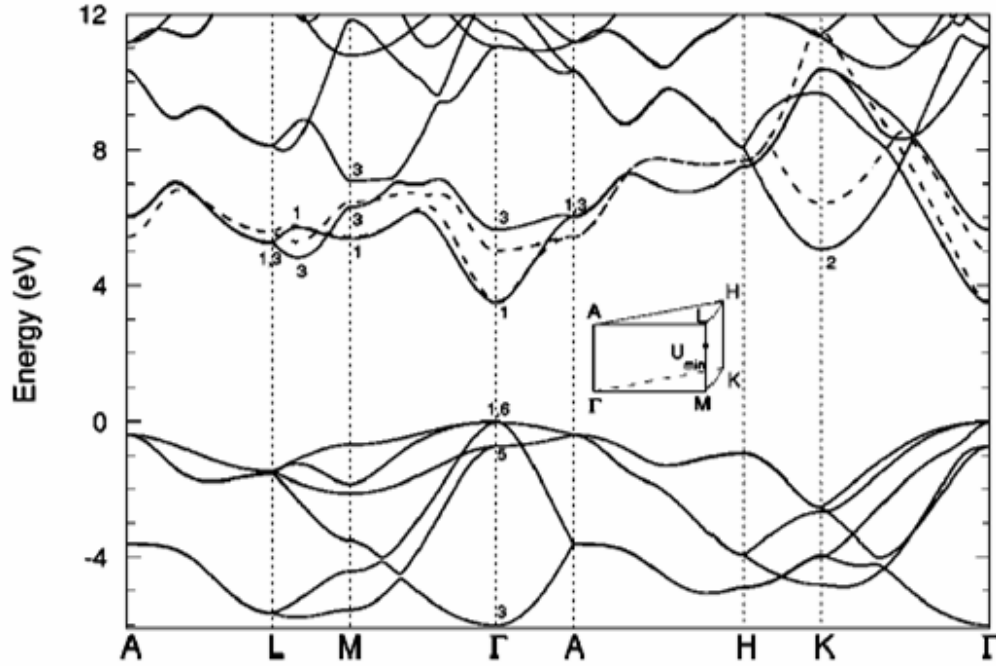


Figure 1.1: Wurtzite GaN band structure calculated using empirical pseudo-potential method – [7].

An observation of this phenomenon has actually been reported by Wraback et al. in 2003 [8]. His time-resolved electroabsorption measurements showed (pump-probe experiments) that even at 130 kV/cm electric field strength, which is below the very *optimistic* 150 kV/cm electron transfer threshold – we believe it to be 300 kV/cm, velocity overshoot is observed. Above the threshold field, overshoot happens due to intervalley transitions -- electrons being transferred to the  $\Gamma$  valley where they are heavier and thus slower. Overshoot happening below the transfer threshold field is most likely due to band nonparabolicity, namely related to a negative electron effective mass. This conclusion was also supported by Monte Carlo simulations reported by the same authors.



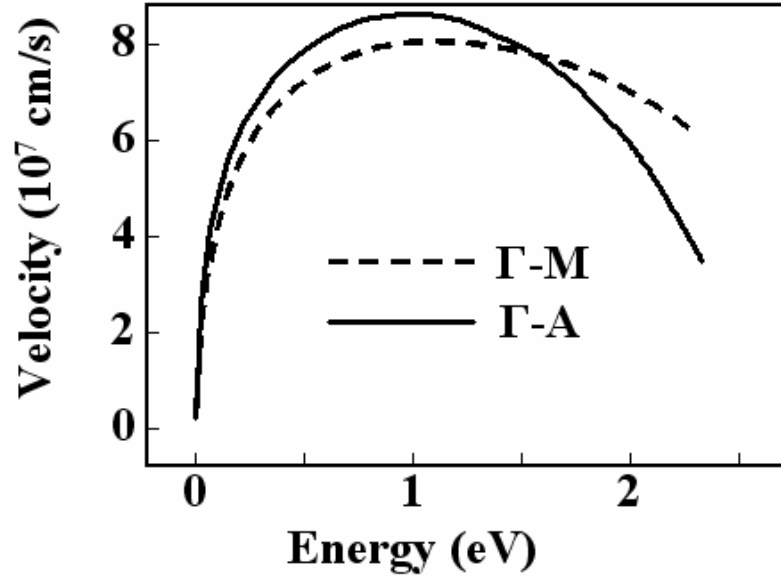


Figure 1.2: Group velocity vs. electron energy in wurtzite GaN.

Going back to the negative mass device prospects, the inflection point is also at a safe distant from the upper valley in addition to transit time of electrons using this material is short enough to prevent electron transfer. Not only electron transfer but also L.O.P phonon emission is also detrimental to the operation of such a device since it alters the direction of the electron (and loose 92 meV energy). Therefore, it is reasonable to expect some transit time restrictions related to this L.O.P scattering rate. This makes a strong electric field even more crucial for the harnessing the phenomena since higher fields will cause a faster acceleration to the inflection point energy according to  $dk / dt = \hbar F$ .

To compare GaN to GaAs in this context, one can say that, as a result of 1.43 eV GaAs band gap and small energy separation between the valleys, intervalley transitions will take place before negative mass effects, if any. Also the same bandgap

will limit the bias field that can be put across the device. As a result, one can only make NDR devices based on intervalley transitions using GaAs and the fastest reported is third harmonic extraction at 108 GHz [9].

Phonon build-up is another possible mechanism that causes velocity reduction in GaN. This has been studied extensively in theory and confirmed by experiments on HEMTs [10-13]. It can even be speculated to play a role in Wraback experiments explaining the peak velocity reduction as the field is increased. The simplest way to look at this phenomenon demands us to think of the phonon dispersion curve. L.O phonons are almost stationary since the slope of this curve is proportional to the group velocity and is pretty flat. Therefore, as a result, in the high field transport regime, the density of these phonons can be significant and they are picked up by the incoming electrons (scattering them) and reduce the average speed of the electrons in the direction of current. This is an import question in the operation of the quasi ballistic horizontal diode and will be addressed in CHAPTER 4.

### **1.3 Negative Differential Conductivity Devices**

There are two types of NDR diodes. First category operates based on a negative-differential-resistance region in its I-V characteristics. If properly terminated and tuned with an inductive reactance, one can set these circuits into stable oscillations ignited by noise which grows exponentially, since there is always a parallel capacitance  $C_D$  associated with these devices. Resonant Tunneling Diode is a good example of this kind.

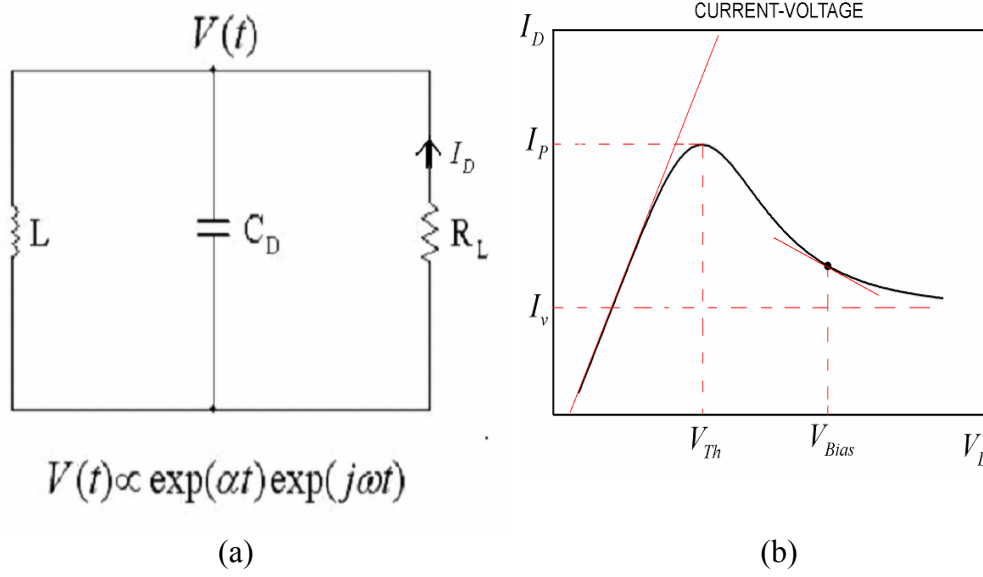


Figure 1.3: (a) Circuit schematics representing an NDR oscillator. (b) Typical I-V characteristics of an NDR diode.

The second type relies on internal space-charge instabilities induced as a result of negative-differential-mobility (NDC) exhibited in the material's velocity-field characteristics. These space-charge instabilities are created basically as a result of the negative effective dielectric relaxation time. This constant being negative causes any disturbance in the space-charge neutrality to grow exponentially instead of dampening as would be in regular materials. These devices too have a parallel capacitance associated with them and need a proper termination and inductive loading to stabilize the oscillations. However, the frequency of oscillations is mainly determined by the transit time of the dipole domains (space-charge instability) and the external circuit has to be tuned around this frequency for proper operation. GaAs Gunn Diodes is an example. Our negative-mass diode belongs to the first category. A THz resonator is required to force oscillations in that frequency range. On the other hand, the semi-ballistic horizontal diode is a transit time device based on space-charge instabilities. This will be detailed in CHAPTER 4.

## CHAPTER 2

# Negative Effective Mass Diodes: Theory and Experiments

### 2.1 Physics of Negative Effective Mass Negative Differential Conductivity

The theory of GaN based Negative effective mass BEAN diode has been studied extensively by *Ridley et al.* for its potential in THz signal generation [14-17]. This chapter is an extended summary of his cited publications. The idea was to introduce a simple model band structure into a classical model of vacuum diode [18], describing the electrical properties and perform a small signal analysis in order to calculate the impedance components, assuming the transport is ballistic. In his treatment, electrons are thermionically emitted over an AlGaN barrier into an intrinsic region of GaN and state  $k_0$ , and are accelerated into negative-effective-mass quantum states under the influence of a very high applied field in order to achieve NDC. Here in this section, we will skip the details of these derivations and focus on the results.

The problem was set up using the following assumptions;

- The diode is modeled as a one dimensional crystal of length  $L$ .
- The diode is assumed to be short enough and the accelerating electric field strong enough for the transit time to be *less than the scattering time* so that the *transport is ballistic*.
- Electrons are injected at the cathode directly into a high-energy state  $k_0$  of the conduction band.

The injection assumed to be via thermionic emission over, or tunneling through, a barrier and therefore the perpendicular component of  $k_0$  is neglected. The presence of

other bands and valleys into which the electrons can scatter are ignored thus only the conduction band is assumed.

### 2.1.1 Ideal Case

In large band-gap semiconductors, where the influence of the valence band in particular is weak, the band along the field direction can be approximately described in terms of a simple cosine function:

$$E = E_0(1 - \cos ka) \quad (2.1)$$

This is a good approximation for GaN, and in fact, plays the key role in allowing such an analytical treatment of the problem rather than having to deal with numerical solutions.

The analysis basically assumes that the total current density in the intrinsic GaN region is composed of a direct-current (dc) and a radio-frequency (rf) component:

$$j_T = j_D + j_s e^{j\omega t} \quad (2.2)$$

Where the amplitude  $j_s$  is assumed to be a constant with respect to time.

Existence of this current density implies the existence of a small signal rf voltage at the terminals of the diode atop the dc bias voltage. One can then calculate the resulting *rf* impedance of the diode as:

$$Z = \frac{V_s}{j_s} \quad (2.3)$$

Real part of which is the *differential resistance* that we are in search of.

This is accomplished by integrating the electric field through out the diode to obtain the potential difference between the terminals of the device as;

$$V = V_D + V_s e^{j\omega t} = -\int_0^L E dx = \frac{\hbar}{e} \int_0^L \dot{k} dx \quad (2.4)$$

Using Brillouin Zone acceleration law which relates the electric field to the wave vector;

$$\dot{k}(x, t) = \frac{e}{\hbar} E(x, t) \quad (2.5)$$

This allows us to linearly relate  $V_s$  to  $j_s$ , using the Llewellyn equation (2.6), and thus to calculate the differential resistance as a function of the applied field  $E_0$ , the dc current component  $j_D$ , the transit time  $T$  and the rf frequency  $\omega$ .

$$\hbar \frac{d^2 k}{dt^2} = e \frac{j_T}{\varepsilon} \quad (2.6)$$

However, the integral is in space and needs to be converted into one over time. This is accomplished through the integration of the group velocity;

$$v_g = (E_0 a / \hbar) \sin k(t) a \quad (2.7)$$

One can transform the integral in (2.4) into one in space,  $x$ .

$$x = x_D + x_{s0} e^{j\omega t} = \int_0^T v_g dt \quad (2.8)$$

This is actually where the simplified band structure comes into the analysis.

The Llewellyn equation follows directly from the analysis below. The total current density  $j_T$  is given by;

$$j_T = \rho v + \varepsilon \frac{\partial E}{\partial t} \quad (2.9)$$

Where,  $\rho$  is the space-charge density,  $v$  is the velocity,  $\varepsilon$  is the permittivity of GaN and  $E$  is the local electric field as a function of space and time. In general, we would also have a *conduction current* component due to the conduction of intrinsic carriers in the material but we assume it is negligible. Since we can express  $\rho$  in terms of the electric field through the Gauss's Law, we have;

$$j_T = \varepsilon \left( v \frac{\partial E}{\partial x} + \frac{\partial E}{\partial t} \right) \quad (2.10)$$

Using total differentials we have,

$$dE = \frac{\partial E}{\partial x} dx + \frac{\partial E}{\partial t} dt \rightarrow \frac{dE}{dt} = \frac{\partial E}{\partial x} \frac{dx}{dt} + \frac{\partial E}{\partial t} = \frac{\partial E}{\partial x} v + \frac{\partial E}{\partial t} \quad (2.11)$$

Substituting (2.10) in (2.11) we can conclude;

$$j_T = \varepsilon \frac{dE}{dt} \quad (2.12)$$

Again, using the acceleration law we have,

$$\frac{dp}{dt} = \hbar \frac{dk}{dt} = eE \quad (2.13)$$

Taking the time derivative of both sides of (2.13) and using (2.12) we have,

$$\hbar \frac{d^2 k}{dt^2} = e \frac{dE}{dt} = j_T \quad (2.14)$$

Going back to the main results, the real part of the impedance  $V_S/j_S$ , the *differential resistance*, is given by:

$$R = R_B \frac{1}{\omega^2 \omega_B (\omega^2 - \omega_B^2)} [\omega_B (\cos y + \cos \alpha) (1 - \cos \omega T) - \omega (\sin y - \sin \alpha) \sin \omega T] \quad (2.15)$$

And the reactive part is:

$$X = -\frac{L}{\varepsilon \omega} - R_B \frac{1}{\omega^2 \omega_B (\omega^2 - \omega_B^2)} \times \begin{bmatrix} \omega_B (\sin y - \sin \alpha) (1 + \cos \omega T) \\ -\omega (\cos y + \cos \alpha) \sin \omega T \end{bmatrix} \quad (2.16)$$

Where  $T$  is the transit time,  $\omega_B = eE_0 a / \hbar$  (Bloch frequency),  $y(t) = \omega_B (t - t_0) + k_0 a$ ,  $R_B = (ev_m a / \varepsilon^2 \hbar) j_D$  and  $\alpha = k_0 a$ .

In a small-signal approximation, all rf components are taken as small compared with the dc components. The relative magnitude of the dc components is determined by the amount of space-charge injected. If this is large, the applied field at the cathode will be reduced almost to zero, in which case, the current will be space-charge limited. The opposite case is when the field is so large that the effect of the injected charge is negligible. This latter case is the one of principal interest initially. The results of the more complex general case will be presented shortly, but for the ideal case, the effect of space charge on the applied field was assumed to be negligible as presented in the results of (2.15) and (2.16).

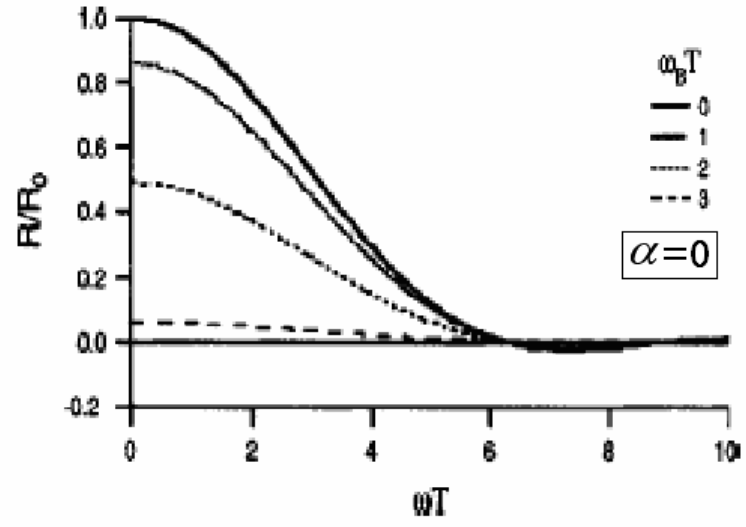


The differential resistance given in equation (2.15) is plotted as a function of the frequency  $\omega$  in Figure 2.1. and, comparing plots in (a) and (b), it is observed that ‘hot’ injection is necessary in order to achieve negative differential resistance (NDC). In Figure 2.1a, one can see that as  $\omega BT$  is increased, the differential resistance is reduced as the resistance due to the states with positive mass is neutralized by states with negative-mass, but it never assumes negative values. In contrast, the case of hot injection leads to a significant NDC as shown In Figure 2.1b stretching from  $\omega=0$  to  $2\pi$ , which corresponds to the frequency bandwidth from 0 to 30 THz.

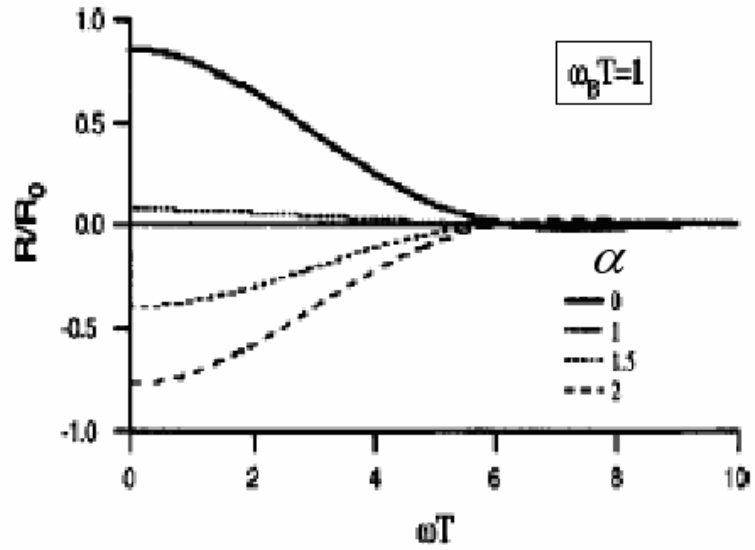
### 2.1.2 Arguments on the Scattering

For effective ballistic motion, the transit time should not exceed the momentum relaxation time (estimated  $\sim 30$  fs) [19] and the displacement current should be taken into account in the calculations. The scattering time associated with this momentum relaxation time is 10 fs. Here, the relevant relaxation time is taken to be that of the momentum since both energy relaxation and intervalley transfer times are roughly an order of magnitude longer, latter being due to the small Bloch overlap function. [7]. In addition, a recent measurement [20] of the scattering time to the L valley has also justified our neglecting by reporting it to be 100 fs. In addition, the lowest valley in GaN is at least 1.4 eV above the conduction-band edge making electron transfer even harder [20].

The 30 fs momentum relaxation time estimation assumes that the principal scattering mechanism in this high-field, high-energy regime is via  $\sim 92$  meV polar-optical-phonon (POP) emission which is an inelastic process.



(a)



(b)

Figure 2.1: Normalized differential resistance as a function of frequency for (a) 'cold' injection (b) 'hot' injection. Figures on the curves refer to the Bloch factor  $\omega_B T$ , where  $\omega_B$  is the Bloch frequency and  $T$  is the transit time. The normalizing resistance  $R_0$  has been chosen to give unity at zero frequency for  $\omega_B=0$  case.

The POP scattering in *wurtzite* GaN is also somewhat anisotropic, however, for simplicity; this was ignored in Ridley et al.'s treatment. In the presence of high fields Zener tunneling into higher lying bands becomes possible as well, but we will assume that this process can be neglected except at extremely high fields. Following these arguments, a diode of 225 Å, a hot injection level of ~360 meV ( $\alpha = 0.75$ ) and a field of 1 MV/cm which gives a transit time of ~25 fs, and therefore has a potential to work. It should be noted here however that the 30 fs momentum-relaxation estimate mentioned above was based on the conventional Fermi Golden Rule, ignoring any intra-collisional field effect and the brevity of the transit time, and this demands more work since fundamental issues that it raises needs to be addressed.

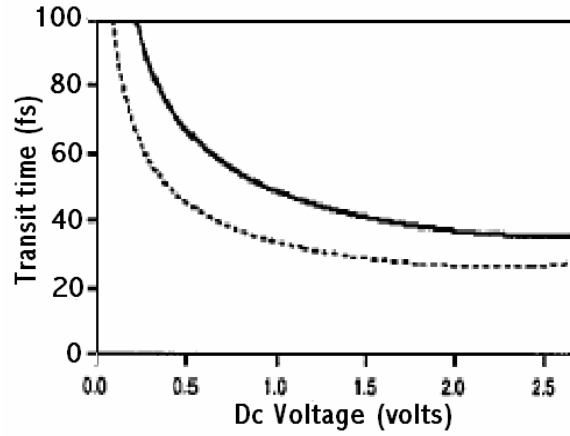
In practice, considering that the scattering times are anywhere between 10 fs to 30 fs, some electrons traversing the short diode will indeed emit a phonon. The idea of the short diode length is to have as few as possible emit. Those that do emit will tend to emit in the forward direction thus minimizing *momentum relaxation*.

### 2.1.3 Space-Charge Limited Case

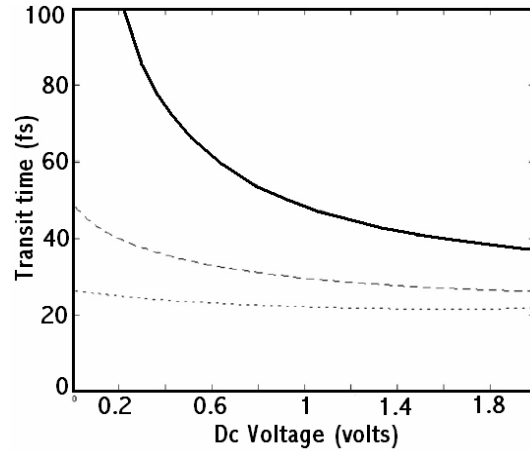
Having established the results of the ideal case (SCL free, perfect ballistic motion), Ridley et al. [16], as the next step, introduced the space-charge effects in his analysis and confirmed that it makes the achievement of ballistic motion more difficult, primarily due to an increase in the transit time as shown in Figure 2.2(a).

The differential resistance curves in the SCL case for various injection levels are shown in Figure 2.3. It is clear from this figure that even *higher* injection energies are necessary to achieve a reasonable NDC. Higher level injection requirement compared to SCL free case accounts for the increase in the transit time as well as giving the

electrons a head-start closer to the negative-effective-mass states (The Inflection point is roughly 1 eV above the conduction band minimum). It should be noted that the dc component of the current through the diode will not show an NDC. It is the rf component that will experience exponential growth. The properly biased diode simply represents a negative reflection coefficient to the load and that leads to rf oscillations.



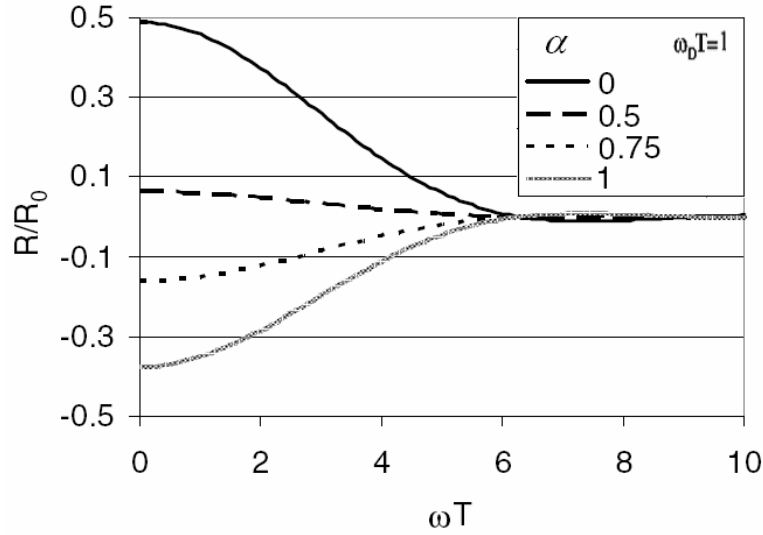
(a)



(b)

Figure 2.2: Transit time vs. voltage for a 20 nm diode. (a) ‘Cold’ injection SCL case (continuous) vs. SCL free case (dashed). (b) ‘Hot’ injection SCL case at various injection levels. Solid line  $\alpha=0$ , long dash  $\alpha=\pi/8$  and short dash  $\alpha=\pi/4$ . In the absence of hot injection the transit time has a strong dependence on the dc voltage. As the level of hot injection increases, the transit time decreases nearly becoming independent of dc voltage at  $\alpha=\pi/4$ .

As the first step in the implementation of this device, we have designed the band diagram (Figure 2.4). In this design, electrons are injected into the intrinsic GaN region at the  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$  interface with an energy equal to the conduction band offset ( $\sim 0.38$  eV). There will of course be an injection energy distribution due to finite tunneling probabilities at every point through the (approximately) triangular barrier above the Fermi level (shown as degenerate), however; majority of the injection is expected to be thermionic.



(a)

Figure 2.3: Differential resistance as a function of frequency for various injection levels (SCL case). The normalizing resistance  $R_0$  is chosen such that the resistance is unity at zero frequency  $\omega_B=0$ .

If enough bias voltage is put across the device terminals, the potential barrier holding the electrons back at the  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  side of the interface can be annihilated, allowing them to spill into the high field region to be accelerated ballistically into the negative effective mass states. The role of the  $n^{++}$  layers on both sides of the intrinsic layer is to facilitate good ohmic contacts to the physical device and providing large number of electrons.

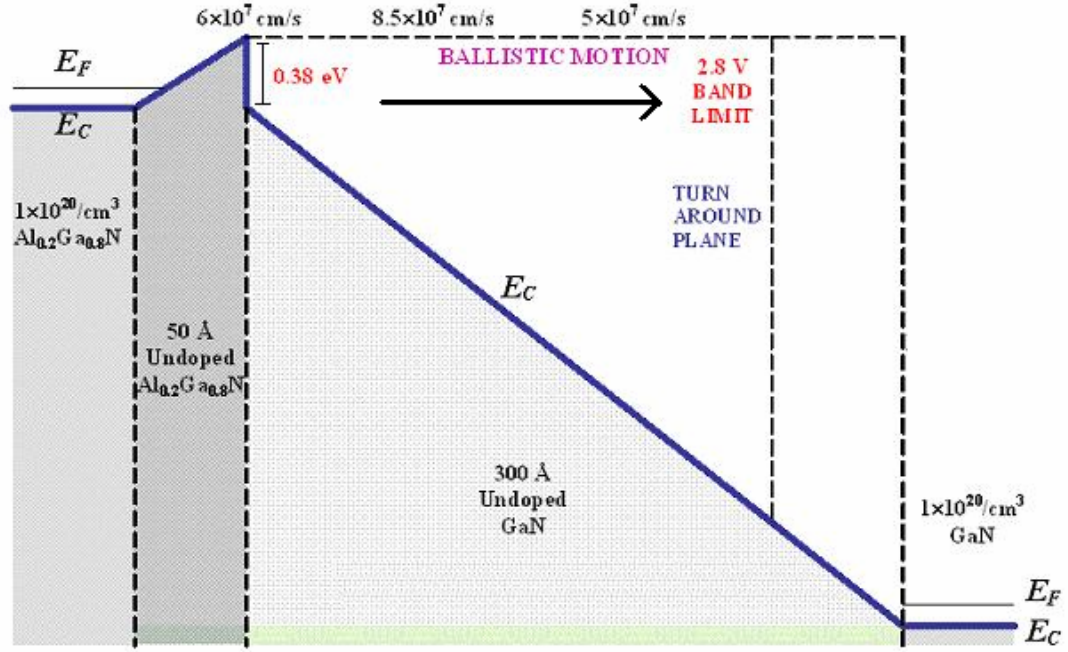


Figure 2.4: BEAN diode band diagram with hot injection. Left is the cathode electrode.

From a practical perspective, the crucial time-constant in the operation of these devices is the *energy-relaxation time*. If it is longer than the transit time, the motion will be *approximately* ballistic - hence diode lengths of 30 – 40 nm are expected to work. Even if momentum relaxation is significant, an NDC will occur provided that energy relaxation is insignificant [16, 21]. In the case of short diodes, there will always be a fraction of electrons that are ballistic. *As long as this fraction dominates, NDC is expected to take place.* Hot injection still plays the key role and helps decrease the transit time. Details of the techniques that were used to fabricate these devices are presented in CHAPTER 3. Before that, we will first discuss the dc/rf measurement set-up and the results obtained with it.

## 2.2 Experimental Results

### 2.2.1 dc Measurement Set-Up

The dc measurement set-up is shown in Figure 2.5. It consists of a probe station, a 4142B modular DC source/monitor, the GPIB interface for ICCAP software (which controls the 4142B) and extra equipment for pulsed measurements.

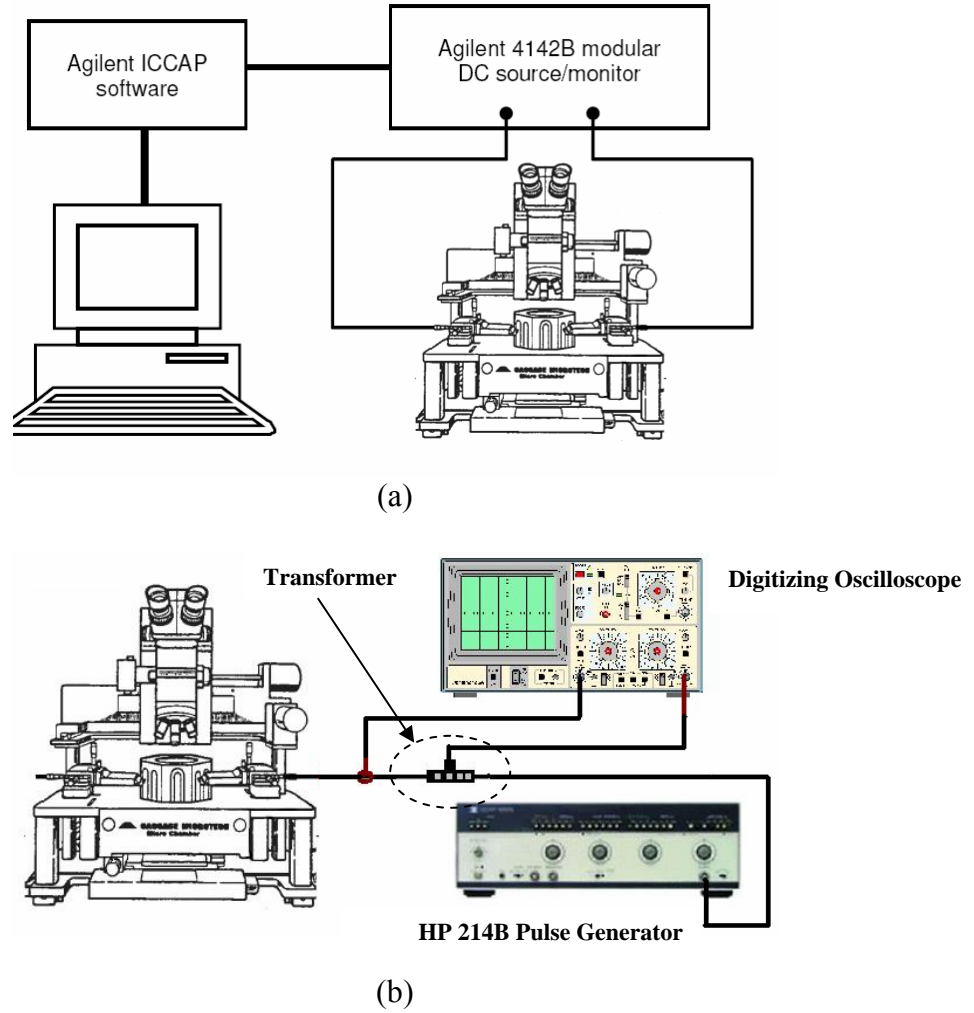


Figure 2.5: dc measurement configuration. (a) CW bias set-up (b) Pulsed bias set-up.

All pulsed bias measurements were performed manually using a pulse generator (HP 214B), a digitizing oscilloscope (HP 54501A) and a current transformer (Figure 2.5b).

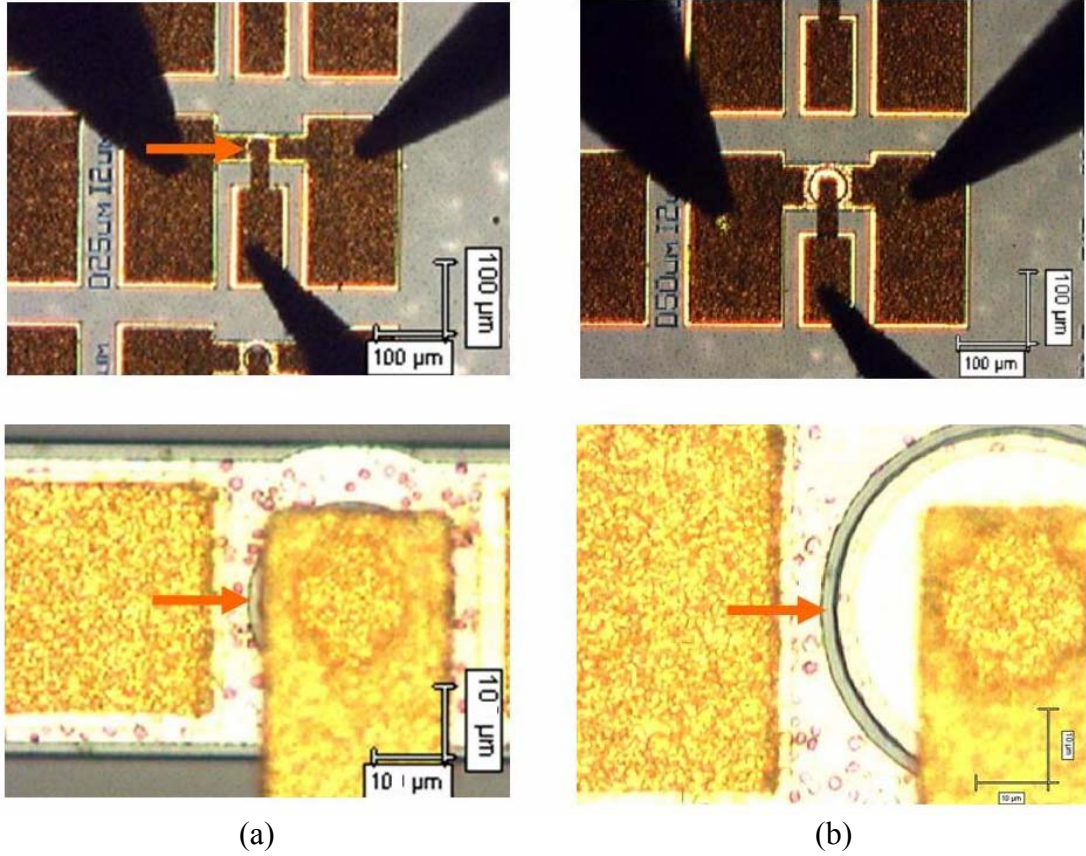


Figure 2.6: Top-view photographs of the devices (air-bridge) during measurements (a) a 5  $\mu\text{m}$  device (b) a 50  $\mu\text{m}$  device

The current and voltage are probed very close to the device under test using appropriate BNC T-junctions. The period of the source is adjusted to the longest possible duration to minimize heating. Next, the device is carefully probed on the station. The voltage on pulse generator is increased until the voltage across the device terminals reaches a target value. Then the current reading is paired with voltage and recorded. For short pulses like  $\sim 150$  ns, ringing effect is quite visible. To ensure the accuracy of the voltage reading, the pulse is made longer briefly to follow the damped ripples to its steady state value.



### 2.2.2 Hot Injection Devices

#### Wafer GS2175

This wafer was grown in the c-plane on a sapphire substrate and epitaxial layers were doped with silicon. The devices were fabricated using the dielectric-bridge technique (3.2.2), namely, the devices were buried under a  $\sim 2 \mu\text{m}$  thick  $\text{SiO}_2$  layer and electrical contact was made through etching the oxide away atop the mesa. Epilayer structure for this wafer is presented in Table 2-1.

Table 2-2, ohmic contact parameters extracted from on wafer TLM measurements are shown. These contacts have been annealed at  $\sim 800^\circ\text{C}$  for  $\sim 30$  seconds.

Table 2-1: Wafer GS2175 epilayers

Epilayer	Thickness (nm)	Doping ( $\text{cm}^{-3}$ )
$\text{N}^+ \text{GaN}$	60	$2 \times 10^{19}$
i – GaN	30	Intrinsic
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	5	Intrinsic
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	20	$2 \times 10^{19}$
$\text{N}^+ \text{GaN}$	1000	$2 \times 10^{19}$

Table 2-2: GS2175 - Measured Ohmic Contact Data (Top Contact)

$R_C$ (ohm-mm)	$R_{Sh}$ (ohm/sq)	$R_{Sp}$ (ohm- $\text{cm}^2$ )	$L_t$ ( $\mu\text{m}$ )
0.57	50	$6.6 \times 10^{-5}$	11.5

Shown in Figure 2.7, is the pulsed-biased I-V measurement of a  $5 \mu\text{m}$  diameter device. A negative differential conductivity (NDC) like behavior is observed as the bias voltage is increased beyond  $\sim 3.5 \text{ V}$ . During these measurements, within the NDC

region of the I-V characteristic, the device was biased at each point for approximately 30 seconds or more; and the I-V point was observed to be stable (time invariant). On the contrary, this was not the case when the destructive power dissipation level was reached. At that dissipation level, the current first rose in amplitude, fluctuated, and then fell down to zero, indicating an open circuit. Therefore, we can argue here that the NDC behavior may in fact be real. However; no indication of high frequency oscillations of any sort was detected such as bias circuit oscillations or a sudden ‘step-like’ drop in the dc current level.

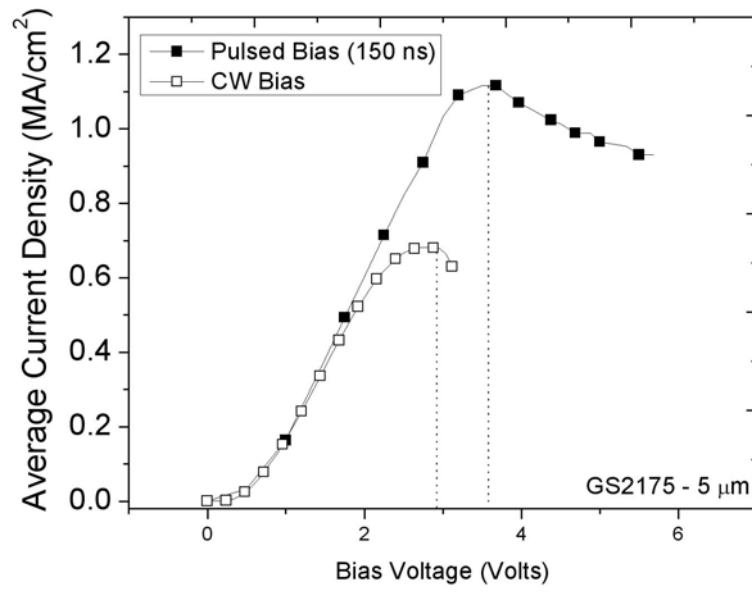
### **Wafer Gs2286**

This sample has been processed twice. First process run failed because top contacts were damaged (partially peeled off) after the second lift-off for the cathode contacts. All of the metal layers on the sample were wet etched using Aqua-Regia for ~3 minutes and the entire process was repeated from the beginning after proper surface cleaning. Also, this wafer was among those on which the self-aligned Ni Mask technique was first tried.

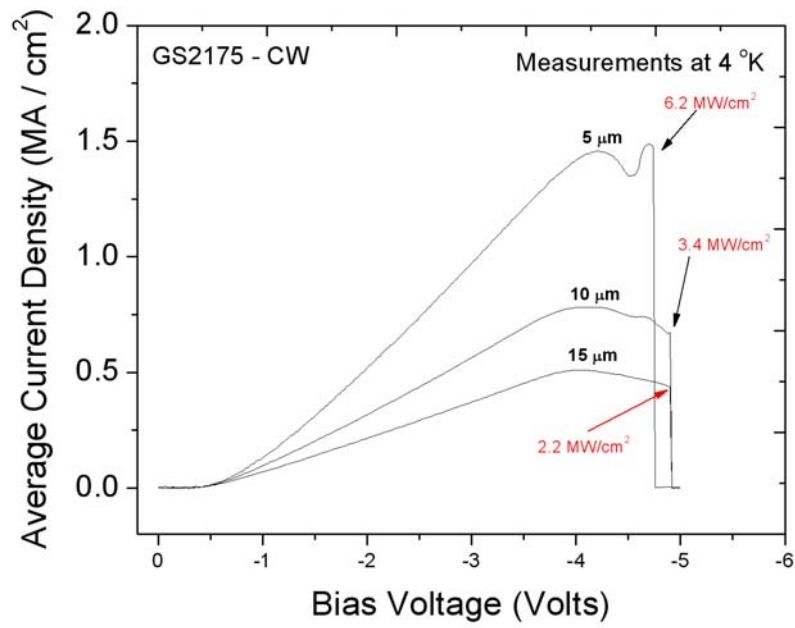
Table 2-3: Wafer GS2286 epilayers

Epilayer	Thickness (nm)	Doping ( $\text{cm}^{-3}$ )
$n^{++}$ GaN	60	$1 \times 10^{20}$
i – GaN	30	Intrinsic
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	5.5	Intrinsic
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	25	$1 \times 10^{20}$
$n^{++}$ GaN	650	$1 \times 10^{20}$

Measured ohmic contact parameters are presented below in Table 2-4. Both specific contact resistance and sheet resistance parameters are very low due to extremely high  $n^{++}$  doping.



(a)



(b)

Figure 2.7: Wafer 2175. I-V characteristic comparison of Pulsed and CW operation.

To achieve self aligned mesa and anode contacts, 120 nm of Nickel was thermally evaporated as a hard etching mask on top of the anode contact stack without breaking the vacuum. Roughly, half of this Nickel layer was consumed during the self-aligned etching process.

Table 2-4: GS2286 - Measured Ohmic Contact Data

$R_C$ (ohm-mm)	$R_{Sh}$ (ohm/sq)	$R_{Sp}$ (ohm-cm <sup>2</sup> )	$L_t$ (μm)
0.0195	11.05	$3.4 \times 10^{-7}$	1.76

Furthermore, the ohmic contacts were not annealed for this wafer. The intention was to eliminate the thermal instability during device operation, previously observed with the non-alloyed Ti/Al/Mo/Au stack, by eliminating aluminum. For this process run, we used Ti (15 nm)/Mo (45 nm)/Au (55 nm) as the ohmic stack.

In Figure 2.8(a), we see the I-V data showing successive voltage sweeps of a random device on the chip. We observe an NDC region in the first sweep and the second sweep produces another NDC region with a slightly higher threshold voltage. The displacement of the threshold voltage of the third NDC region is even more pronounced.

Despite the threshold voltage, the peak current level for these first three sweeps stays almost the same and thus suggesting the following explanation: Each sweep produces extreme joule heating and, as a consequence, increases the anode ohmic contact resistance. This in turn demands more terminal bias to drop the threshold voltage across the intrinsic layer. The fourth and fifth sweeps do significant damage to the contacts that current levels drop.

### Wafer Gs2341

This wafer was grown atop 250  $\mu\text{m}$  thick n-type silicon carbide (SiC). Table 2-5 shows the wafer structure. Note that the top  $n^{++}$  layer was grown thicker than usual ( $\sim 60$  nm) with the concern that the metal protrusions might penetrate into the intrinsic layer after annealing the contacts. References show that this penetration may be as deep as 120 nm.

Table 2-5: Wafer GS2341 epilayers

Epilayer	Thickness (nm)	Doping ( $\text{cm}^{-3}$ )
$n^{++}$ GaN	185	$1 \times 10^{20}$
i – GaN	30	Intrinsic
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	5.5	Intrinsic
$n^{++}$ $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	25	$1 \times 10^{20}$
$n^{++}$ GaN	650	$1 \times 10^{20}$

Both anode and cathode contacts were annealed at  $\sim 800$   $^{\circ}\text{C}$  for 30 seconds. Ti (15 nm)/Al (90 nm)/Mo (45 nm)/ Au (55 nm) metal stack was used. Figure 2.9 shows the -I-V characteristics for both the active diode and an adjacent diagnostic device. In part (a), the I-V characteristic shown belongs to the ballistic region. Here we see that the current rises exponentially with increasing bias and eventually the contacts are burned.

Table 2-6: GS2341 - Measured Ohmic Contact Data

$R_C$ (ohm-mm)	$R_{Sh}$ (ohm/sq)	$R_{Sp}$ (ohm- $\text{cm}^2$ )	$L_t$ ( $\mu\text{m}$ )
0.0195	11.05	$3.4 \times 10^{-7}$	1.76

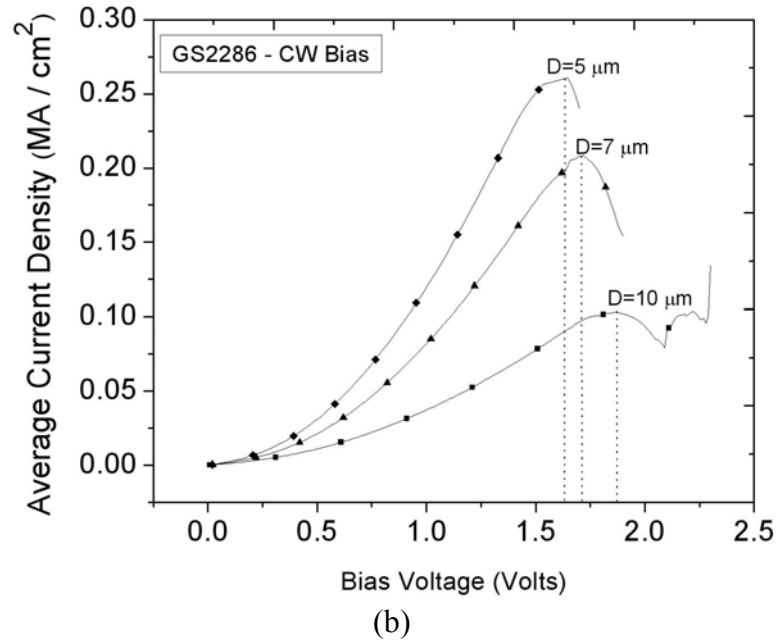
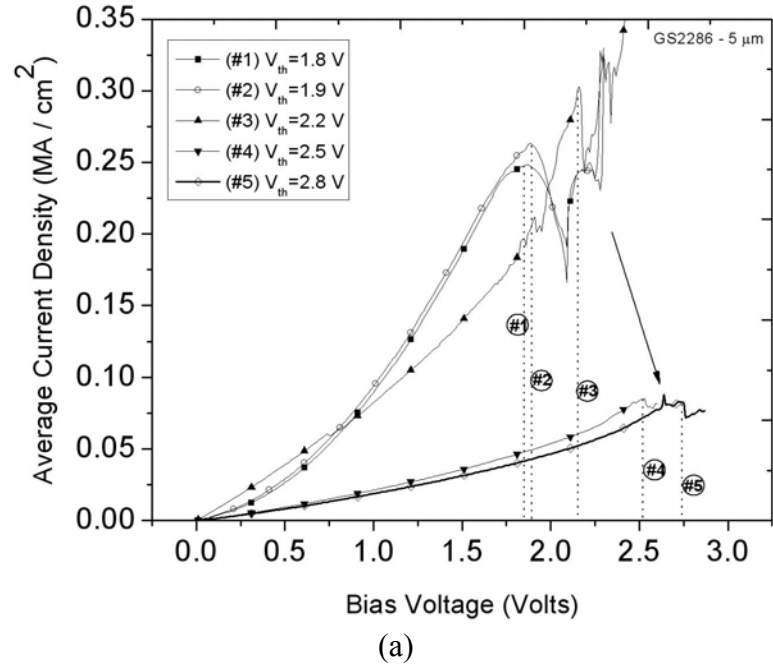


Figure 2.8: Wafer GS2286. (a) Results of a successive CW I-V sweep showing NDC regions. (b) CW voltage sweeps of  $5 \mu\text{m}$ ,  $10 \mu\text{m}$  and  $15 \mu\text{m}$  diameter devices.

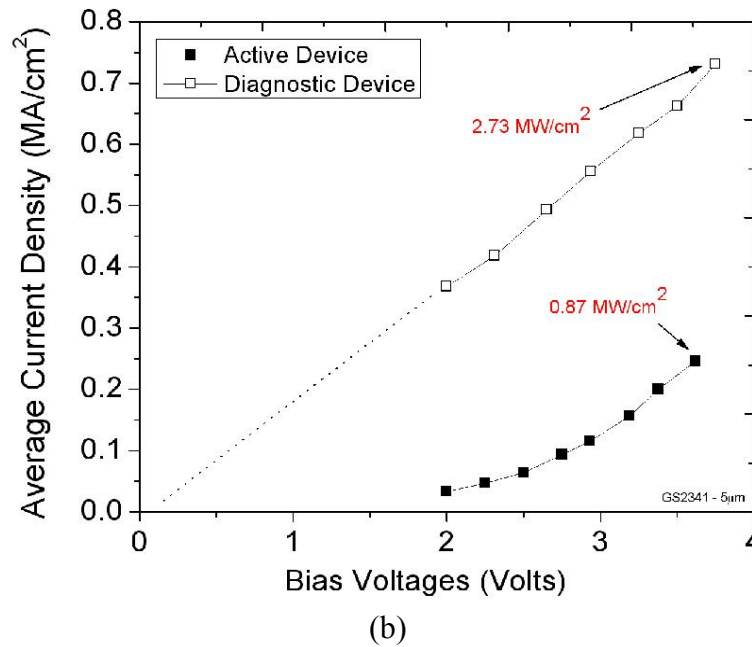
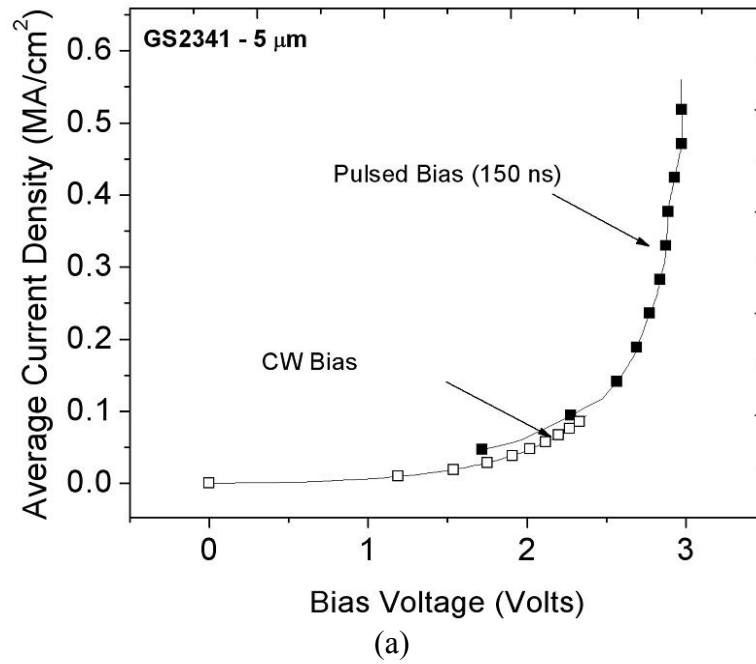


Figure 2.9: Wafer 2341 (a) Current Density vs. bias voltage *across the ballistic region* of a 5  $\mu\text{m}$  diameter device calculated from the raw I-V data shown in part b. This curve compares pulsed and CW biasing conditions. (b) Current Density vs. bias voltage (pulsed) for a 5  $\mu\text{m}$  device and a physically adjacent diagnostic device of same diameter. The dc power level at which the device contacts were destroyed are also labeled.

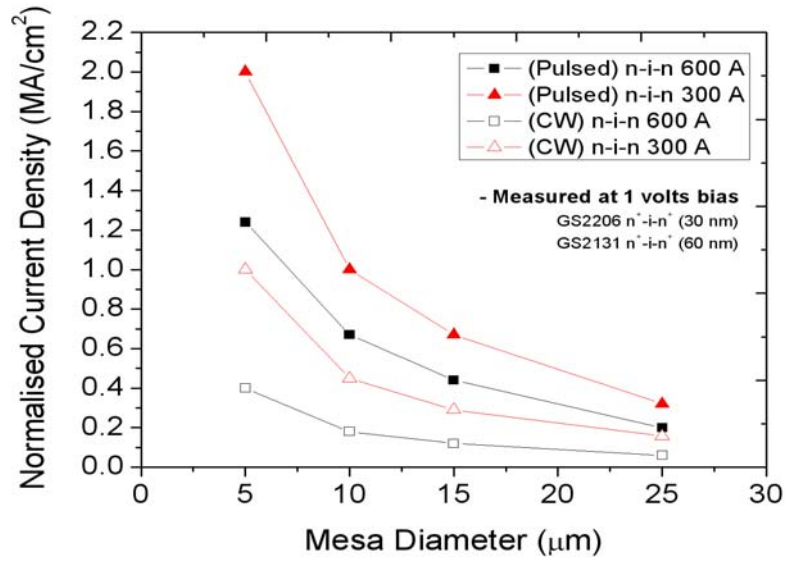
The I-V characteristics in part (a) are calculated by comparing the active device to an adjacent diagnostic device. The result shows that this is the only wafer on which we were able to put an electric field of roughly 1.0 MV/cm across the active region, no indication of high frequency oscillations was observed.

### **2.2.3 Cold Injection Devices**

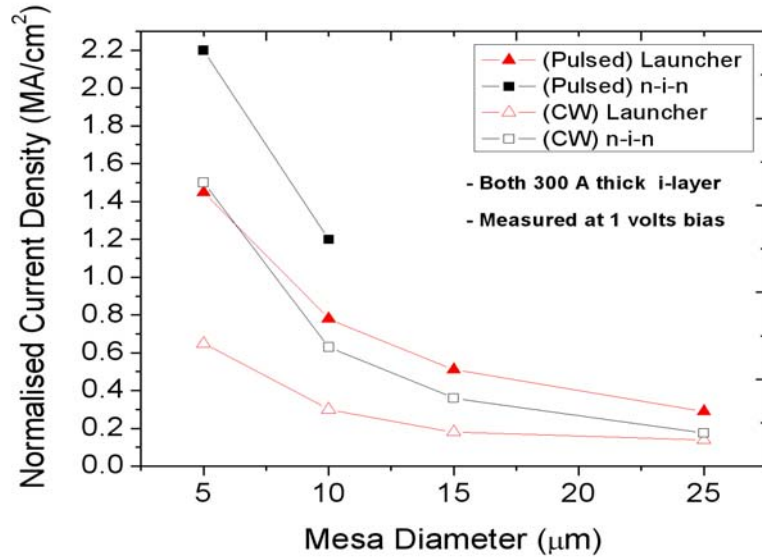
These devices employed an intrinsic layer sandwiched between two highly doped  $n^{++}$  layers of GaN. The main reason behind investigating these structures was to model and compare with Child-Langmuir law to confirm ballistic transport. This approach would demand of course the contact resistivities to be very close on both wafers with different intrinsic layer thicknesses and each device to have extremely low spreading resistance within the device to ensure field uniformity over the entire intrinsic layer.

Figure 2.10a shows a comparison of 30 nm and 60 nm intrinsic layer devices as a function of mesa diameter. The normalized current density is observed to decrease as the diameter is increased. These current measurements are taken at the same bias voltage, 1 volt. This result is understandable since the reduction in resistance with diameter is expected to be faster than that of the area. This curve roughly gives us an idea about the device diameter range that we need to achieve the high current densities required to charge the unit capacitance of the device fast enough for THz operation. In the same figure (Figure 2.10), the increase in total device resistance due to joule heating is also very visible since the curves obtained through pulsed biasing lie well above the ones which were measured with d.c. biasing, indicating higher currents at the same voltage.





(a)



(b)

Figure 2.10: Normalized current density versus mesa diameter (a) Comparison of 5 µm diameter with 30 nm and a 60 nm intrinsic layer thickness (Wafers GS2131 and GS2206) (b) Comparison of 5 µm 30 nm AlGaN launcher device with a 30 nm n-i-n device. All currents are measured at 1 V.

In Figure 2.10b, the 30 nm n-i-n device is also compared to a 30 nm AlGaIn launcher type device. As expected, the barrier in the launcher device band diagram causes the current density to be less than the n-i-n device.

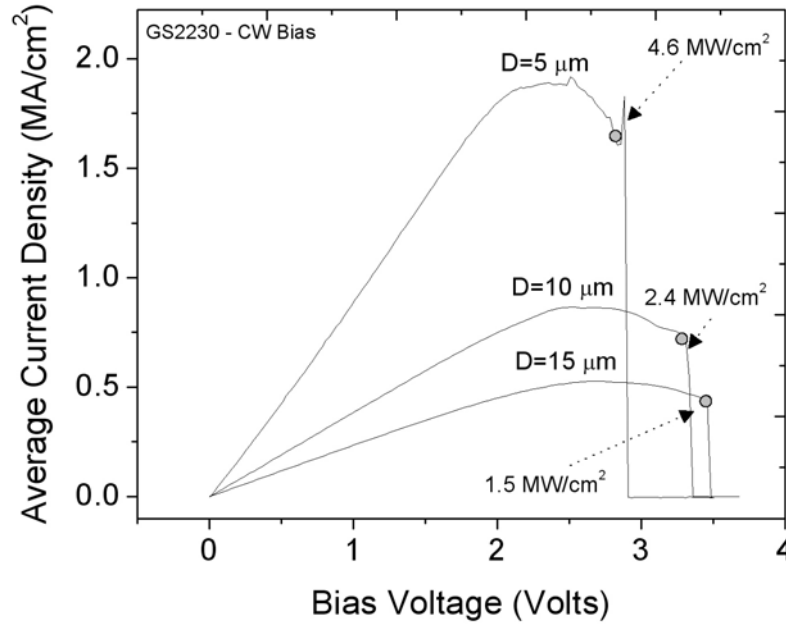


Figure 2.11: I-V characteristics of 5, 10 and 15  $\mu\text{m}$  diameter devices (Wafer GS2230 – 30 nm intrinsic layer). The power density levels at which the devices are permanently destroyed are also marked on this plot.

To look at some individual devices, we plotted measured I-V characteristics of typical n-i-n devices of three different diameters in Figure 2.11. These devices are physically adjacent on the chip, in order to ensure minimum ohmic contact resistance variation. Consistent with the previous discussion, it is observed that the peak current density decreases as a function of increasing diameter. Another observation is that the upper limit of the power density at which the devices are permanently destroyed *decrease* with increasing diameter. This is an indication of the non-uniformity of current across the mesa due to spreading resistance. Current concentrates more around the edges of larger diameters as a result of this resistance.

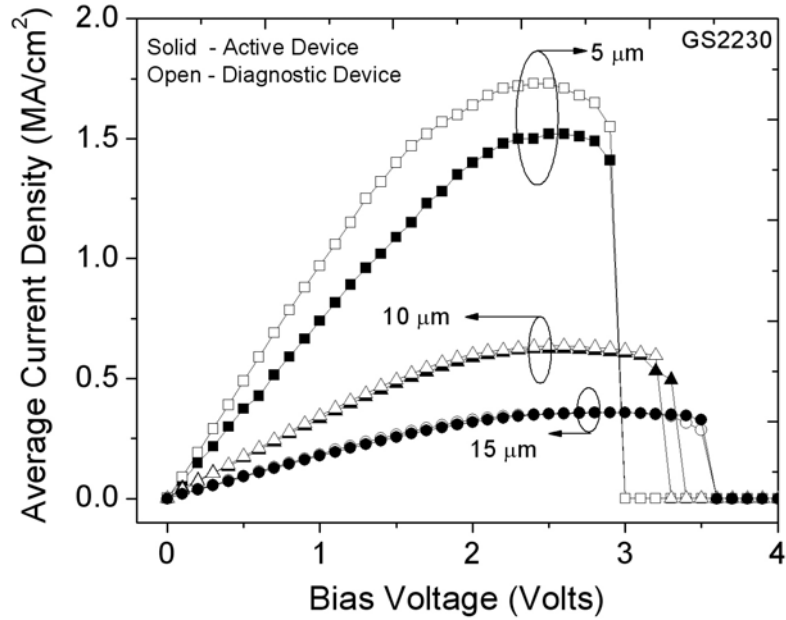
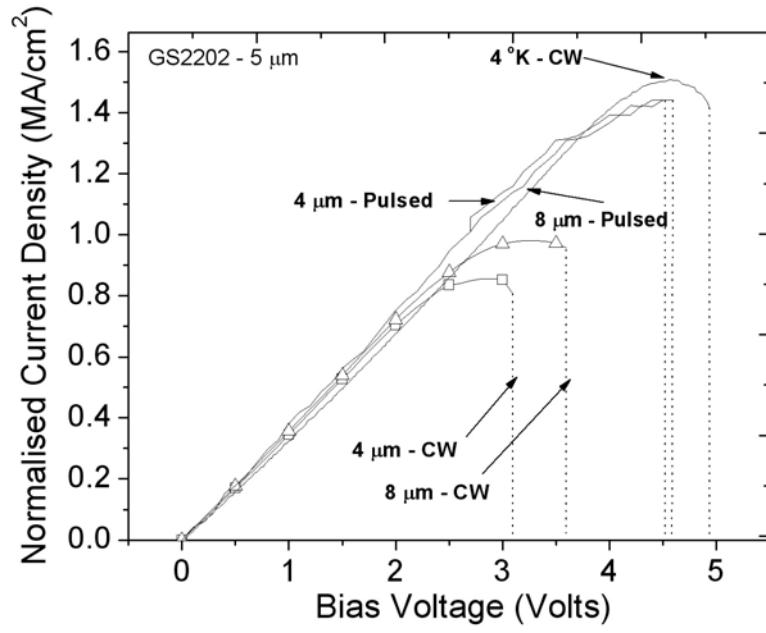
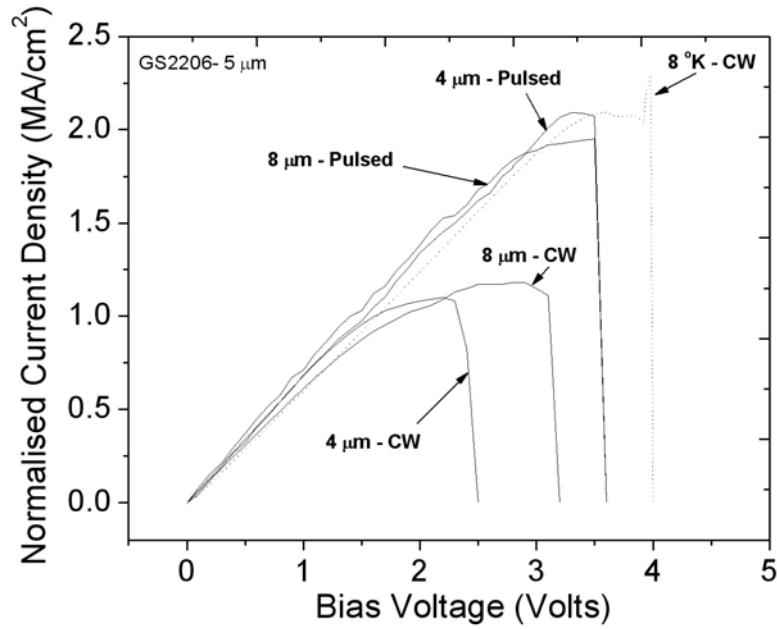


Figure 2.12: I-V comparison of n-i-n devices with their diagnostic counterparts that is physically adjacent on the chip (no mesa structures, roughly representing only the parasitic resistivities)

Experiments were also designed to investigate and push this limit further by improving heat removal or less d.c. power dissipation. In Figure 2.13, I-V characteristics for two different intrinsic layer thicknesses are presented with 4  $\mu\text{m}$  and 8  $\mu\text{m}$  thick air-bridges under CW and Pulsed biasing conditions. Here we see the net effect of pushing this limit of permanent destruction to higher bias voltages as a result of better heat removal and less power dissipation, however; no interesting nonlinear I-V effect is observed before reaching that point. The kinks seen in these graphs are random and artifacts due to manual pulsed bias measurements.



(a)



(b)

Figure 2.13: CW and Pulsed bias I-V characteristics of 4  $\mu\text{m}$  and 8  $\mu\text{m}$  thick 5  $\mu\text{m}$  diameter air-bridge devices. Measurements at 8 and 4 K<sup>o</sup> CW bias are also included (a) Wafer GS2202 – 17 nm (b) Wafer GS2206 – 30 nm.

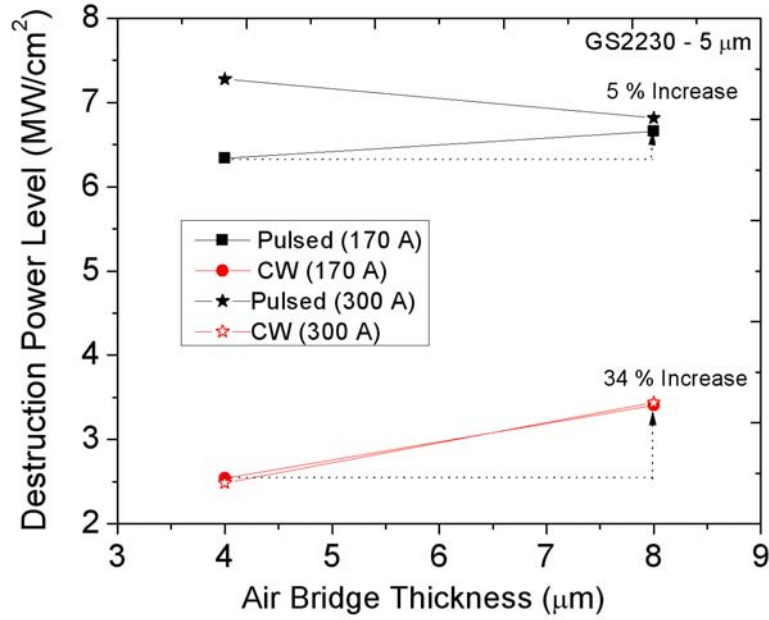


Figure 2.14: Destructive Power Density vs. air-bridge thickness characteristics.

To take a closer look at the dc power dissipation ceiling of these devices, we organized some of the data in Figure 2.14 for a 5  $\mu\text{m}$  device to plot these power levels as a function of air-bridge thickness. Both 30 nm and 17 nm devices are compared under both pulsed and CW biasing. It was observed that *the percentage increase in the power limit as a result of the increase in air-bridge thickness is larger for CW case compared to Pulsed bias conditions*. Another observation is that *the power limit is almost doubled in the Pulsed case compared to CW*. In Figure 2.15, I-V measurements taken at different ambient temperatures of 5 and 15  $\mu\text{m}$  devices are shown. The variation is observed to be significantly more pronounced for the 15  $\mu\text{m}$  diameter device compared to 5  $\mu\text{m}$ .

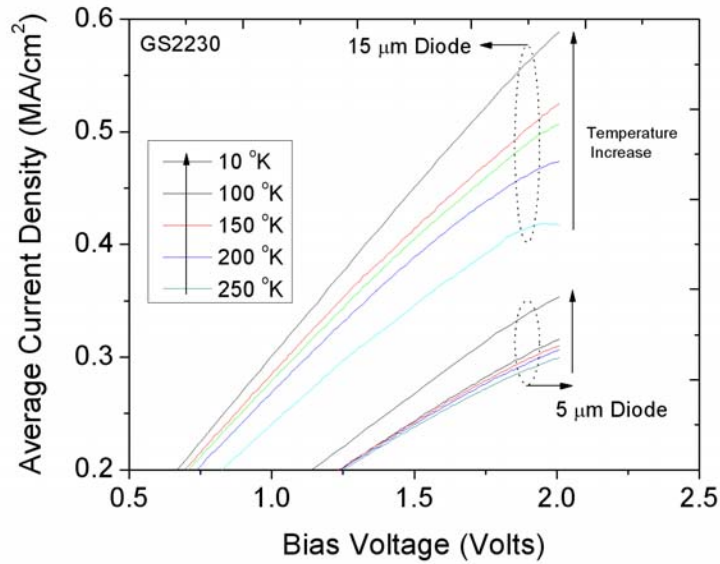


Figure 2.15: The variation of the on-resistance as a function of increasing ambient temperature (Wafer – GS2230). These measurements were taken on a chuck in vacuum. Needle probes were used for electrical contact.

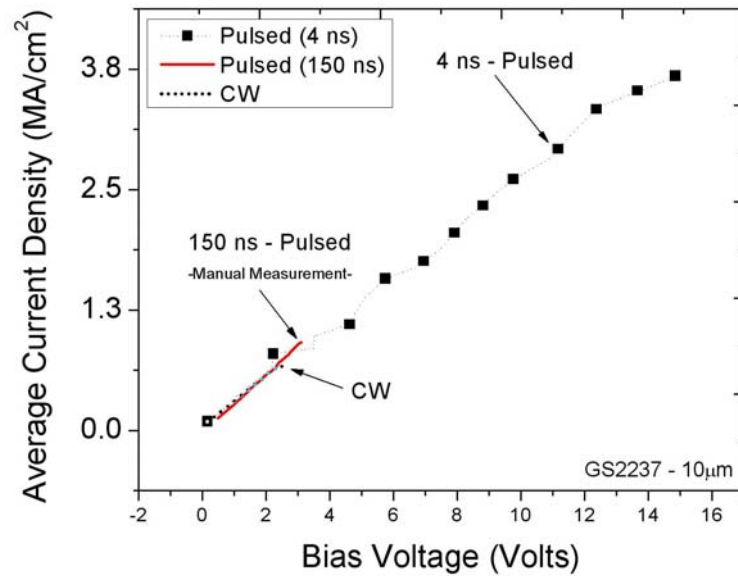


Figure 2.16: Comparison of CW, short (150 ns) and ultra short (4 ns) pulsed biasing I-V characteristics of a 10  $\mu\text{m}$  device. (Wafer GS2237). Ultra-short pulsed device stays roughly the same on-resistance curve up to 14 volts bias. These (4 ns) measurements were taken at room temperature at the Semiconductor Physics Institute, Lithuania.

We have also performed Raman temperature measurements on these diodes. The temperature as a function of the device input-power is shown in Figure 2.17. Smaller diameters were way too hot to measure. These two relatively large diameter devices show the significance of the heating problem.

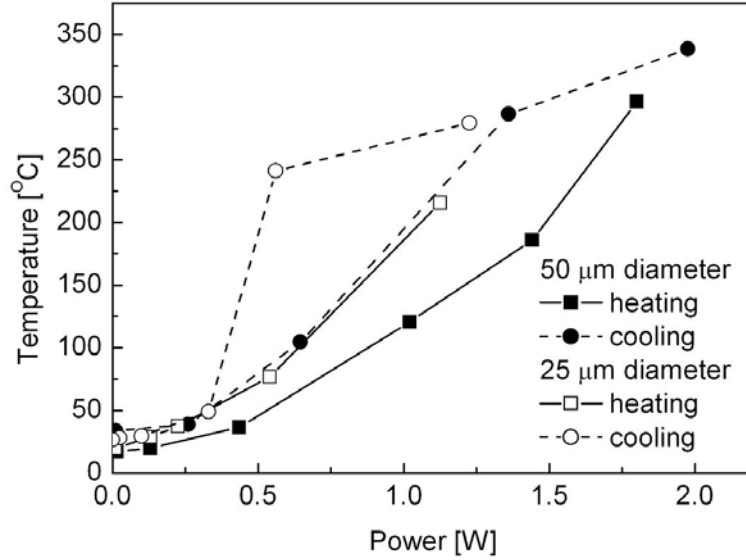


Figure 2.17: Raman temperature measurements as a function of power dissipation. The graph shows the temperature measurements for both directions of power dissipation. Rapid temperature rise is primarily attributed to the low thermal conductivity of the sapphire substrate.

#### 2.2.4 Parasitic Modeling

We have constructed a simple analytical model to study the total parasitic resistance and current density as a function of diameter. Figure 2.18 shows these expressions plotted for a specific set of parameters.

In this section, we will briefly derive the equations that make up our basic parasitic resistivity models whose predictions will be compared to experimental data later on. The dominant component of the total parasitic resistance is that of the anode contact. By definition, given the *specific resistance* in  $\text{ohm-cm}^2$ ,  $R_T$  can be calculated as;

$$R_T = \frac{r_c}{A} = \frac{r_c}{\pi r_1^2} \quad (2.17)$$

Where  $r_1$  is the radius of the active mesa.

Moving on to  $R_A$  (Figure 2.18), with reference to Figure 2.19a, the *conductance* of the ring of thickness  $dr$ , at a distance  $r$  from the center, can be calculated as  $2\pi r/R_{SH}$ . Then, we integrate the *reciprocal* of this function, which is the resistance of the ring, in the direction of the current flow (with respect to  $r$ ), to calculate the total resistance (each of these differential elements are in series with each other in the direction of the current flow)

$$R_A = \int_{r_1}^{r_2} \frac{R_{sh}}{2\pi r} dr = \frac{R_{sh}}{2\pi} \ln \left[ \frac{r_2}{r_1} \right] \quad (2.18)$$

Here,  $r_1$  is the radius of the active mesa where as  $r_2$  is the radius at which current enters the anode. To derive the ohmic contact resistance of the anode electrode, we refer to Figure 2.19b. Using the definition of the transfer length  $L_t$ , we obtain;

$$R_{Lower} = \frac{r_c}{2\pi L_t r_2} \quad (2.19)$$

Where  $r_c$  is the *specific contact resistance* and  $L_t$  is the *transfer length*. A more sophisticated result for the same geometry is derived in [22], which also develops a technique to use planar version of this same geometry for circular transmission line method (CTLTM) ohmic parameter extractions.



The total parasitic resistance of the diode is given by;

$$R = R_a + R_b + R_c = \frac{r_c}{\pi r_1^2} + \frac{r_c}{2\pi L_t r_2} + \frac{R_{sh}}{2\pi} \ln \left[ \frac{r_2}{r_1} \right] \quad (2.20)$$

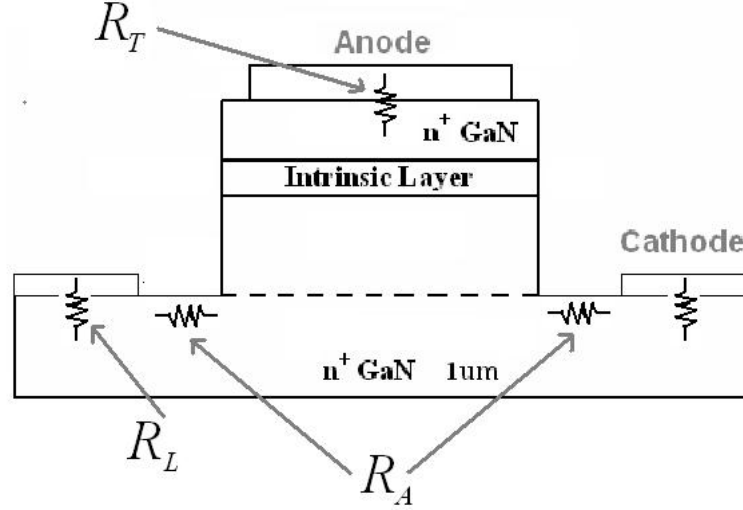
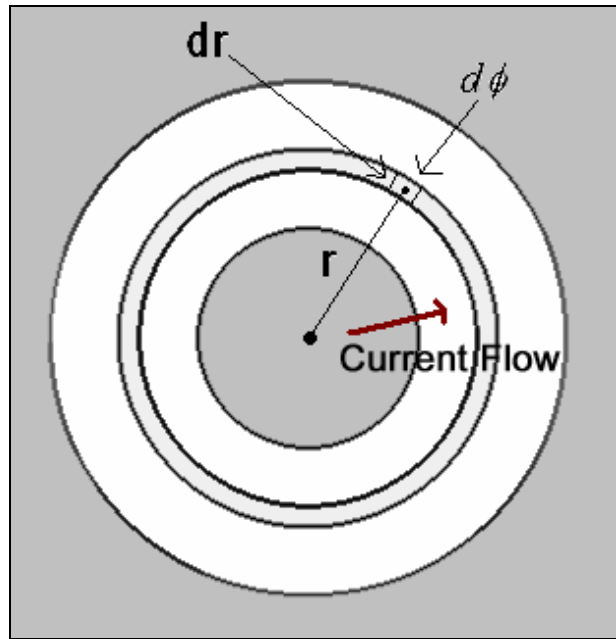
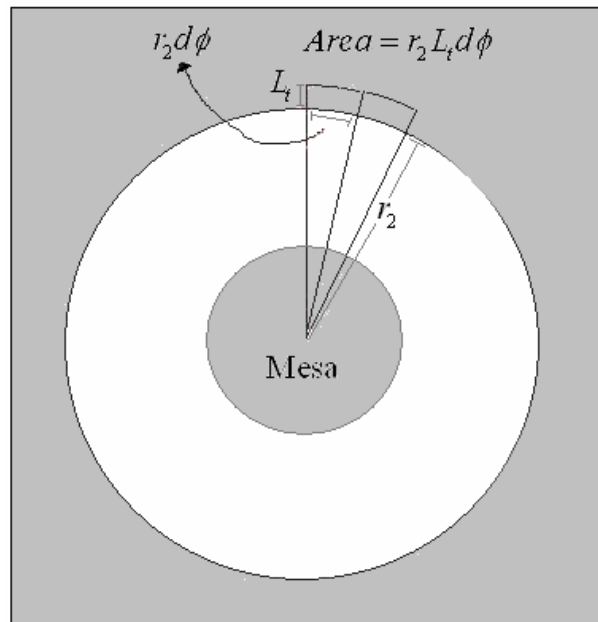


Figure 2.18: Model for the parasitic resistance components associated with the cylindrical diode structure.  $R_T$ ,  $R_A$  and  $R_L$  indicate the anode contact, annular GaN and cathode contact resistivities, respectively.

Equation (2.20) is plotted in Figure 2.20 as a function of the mesa the diameter, ( $2 \times r_1$ ), with  $V_B = 1$  V and  $r_2 - r_1 = 1.5 \mu\text{m}$  for different specific resistivities. Experimental data is also shown along with it. Pulsed bias and CW measurements are quite in agreement with these predictions at the  $r_c = 1 \times 10^{-6} \Omega\text{-cm}^2$ . The experimental data points are taken at 1 volts bias.



(a)



(b)

Figure 2.19: Graphical representation for calculating the resistance of the annular region. The central gray area represents the base of the vertical mesa. The outer gray area marks the cathode contact.

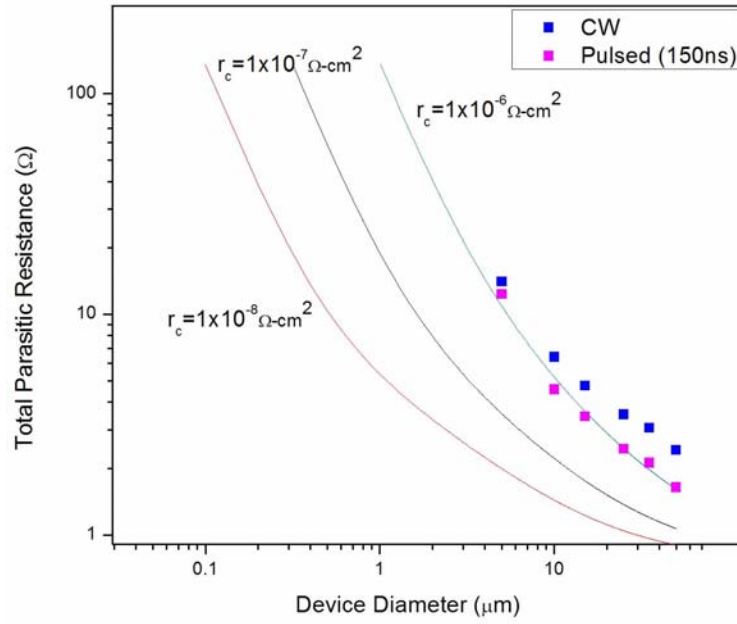
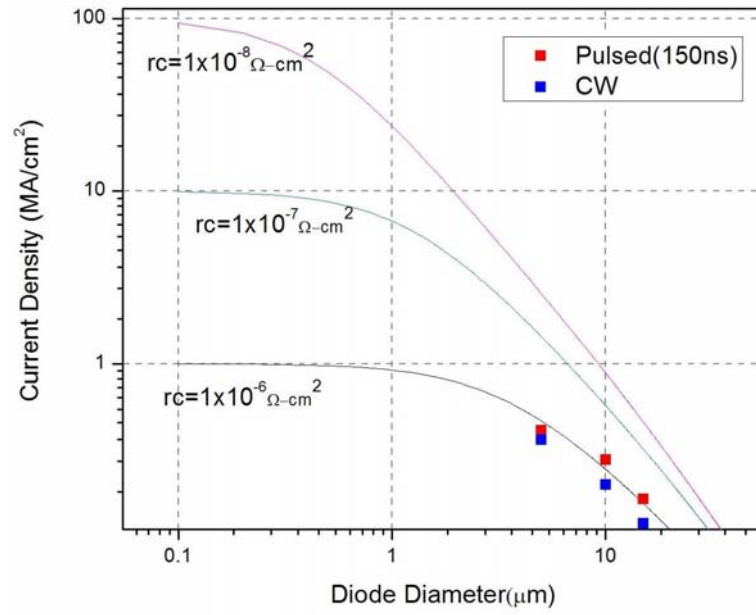


Figure 2.20: Total device resistance curves for different specific resistivities. Experimental data collected under pulsed and CW data (at 1 Volts) is also included.

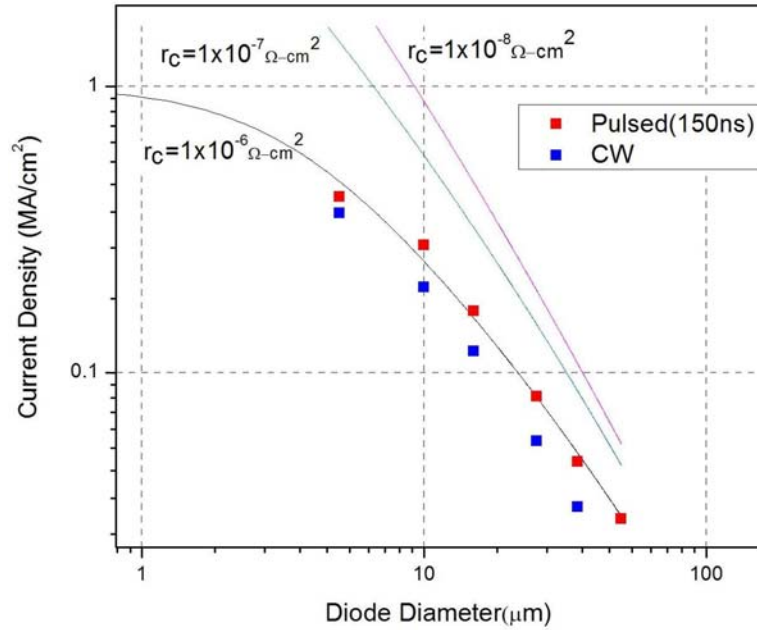
Using Eq. (2.20), we can calculate the average current density using

$$J(r_1) = \frac{[V_B / R(r_1)]}{Area(r_1)} = \frac{V_B}{(\pi r_1^2) R(r_1)} \quad (2.21)$$

Eq. (2.21) is plotted in Figure 2.21 and shown along with experimental data. This plot is particularly useful because it gives us a rough idea about the specific contact resistance and diode diameter range that will allow the high current densities we are seeking for THz operation.



(a)



(b)

Figure 2.21: Calculated parasitic resistivities as a function of device diameter. Discrete square points represent experimental data. Both experimental data and current calculations are at 1 V.  $R_{Sh}=11$ ,  $N_D=1 \times 10^{20} \text{ cm}^{-3}$  and  $t_o=700 \text{ nm}$ . (a) Vertical scale up to  $100 \text{ MA/cm}^2$  (b) Vertical scale up to  $1 \text{ MA/cm}^2$ .

## 2.2.5 Microwave Resonator Design and 2.5D Electromagnetic Simulations

### 2.2.5.1 K-Band Microwave Resonator Design

A K-Band microwave resonator was designed (instead of THz range) to terminate the diode to eliminate the THz measurement complications in the first stage so that the concept can be proven. One port s-parameter measurements were performed to model the diode in terms of its resistive and reactive elements which are needed to design the resonator for a particular frequency.

The resonator design employed a  $\lambda/8$  microstrip transmission line terminated by a  $180^\circ$  *radial stub*. The open ended radial stub with a  $\lambda/4$  radius exhibits an RF short at its input. This is basically a large capacitance due to its large area and the input impedance is almost short for a broad range of frequencies. This RF short becomes a termination to the  $\lambda/8$  line and produces purely inductive impedance at its input. This can be seen from substituting  $Z_L=0$  in;

$$Z_{in}(l) = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \quad (2.22)$$

To yield;

$$Z_{in}(l) = jZ_0 \tan(\beta l) \quad (2.23)$$

For instance, the design for a  $10 \mu\text{m}$  cylindrical diode begins from the capacitance estimation according to the simple model of;

$$C = \frac{\epsilon A}{d} = \frac{0.88 \times 10^{-10} \pi (5 \times 10^{-4})^2}{30 \times 10^{-7}} \cong 0.2 \text{ pF} \quad (2.24)$$

Using this, the capacitive reactance at 30 GHz is;

$$X_c = \frac{1}{\omega C} = \frac{1}{(2\pi)(30 \times 10^9)(0.1984 \times 10^{-12})} = 26.738\Omega \quad (2.25)$$

Is the inductive reactance should be exhibited to the device by the matching circuit.

On the other hand at 30 GHz, the wavelength is  $\sim \lambda_d = \lambda_f / \sqrt{\epsilon_{eff}} = 5.61 \text{ mm}$  in  $\text{SiO}_2$

where  $\lambda_f$  is the free space wavelength and  $\epsilon_{eff} \approx 3.2$  is the effective permittivity.

A microstrip line on  $\text{SiO}_2$  with a  $\sim 26.7\Omega$  characteristic impedance needs to have the dimensions of  $L = 701.21\mu\text{m}$ ,  $W = 9.97\mu\text{m}$ . The design that was optimized using SONNET is shown in Figure 2.22.

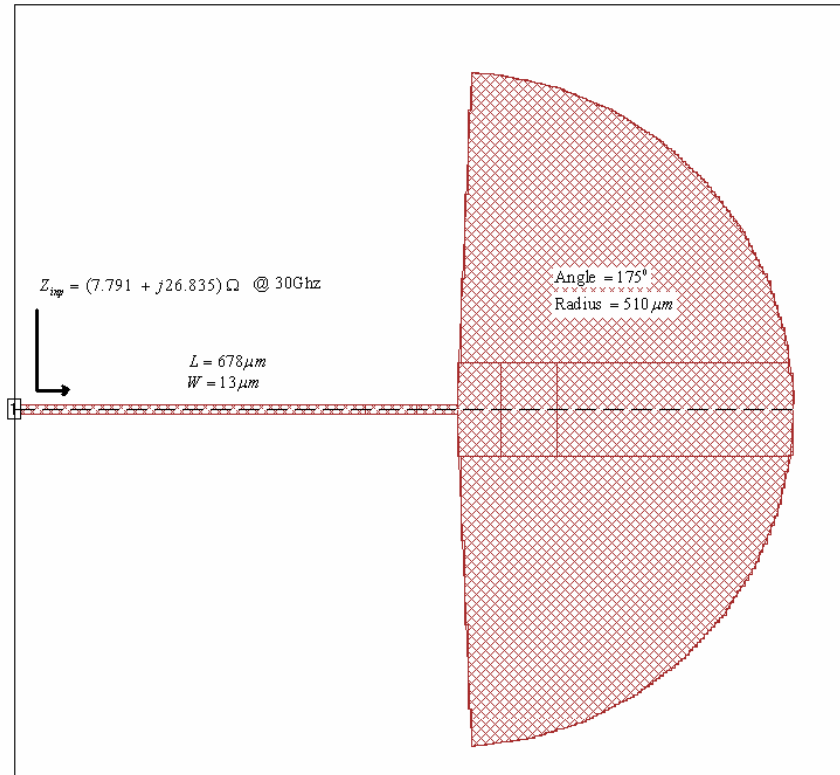


Figure 2.22: SONNET layout of the optimized microstrip resonator structure showing the dimensions and the input impedance.

This SONNET (2.5D passive electromagnetic simulation software) simulation was performed using a very high mesh density at the radial stub/transmission line junction and, at the radial stub edges. This forces the software to use more subsections (method of moment elements) in these areas to make sure that the expected inductive effect is captured in the result. Also vertical symmetry of the of the structure allowed us to simulate only one part and therefore considerably reduced the calculation time.

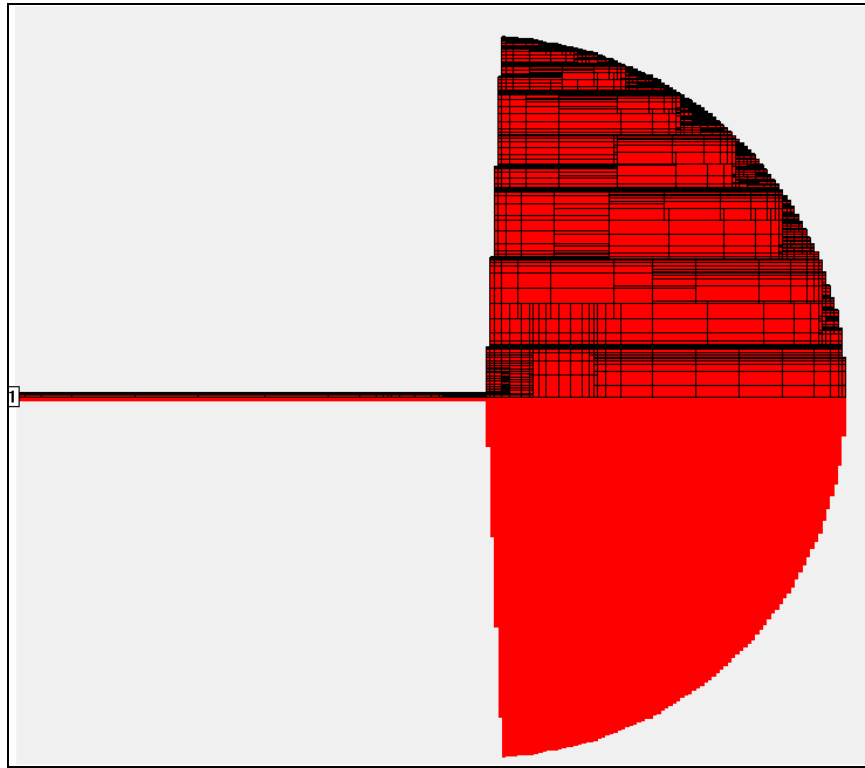


Figure 2.23: Diagram showing the density of the mesh used in the SONNET simulations.

To further speed the simulations, another simplification utilized was to divide the structure in half vertically at the transmission line radial stub junction. This allows the software to ignore the electromagnetic coupling between the two sections during the construction of 2D moment matrix. On the chip, the resonator was implemented using 400 nm thick evaporated gold on 2  $\mu\text{m}$  thick GSI PECVD deposited  $\text{SiO}_2$ .

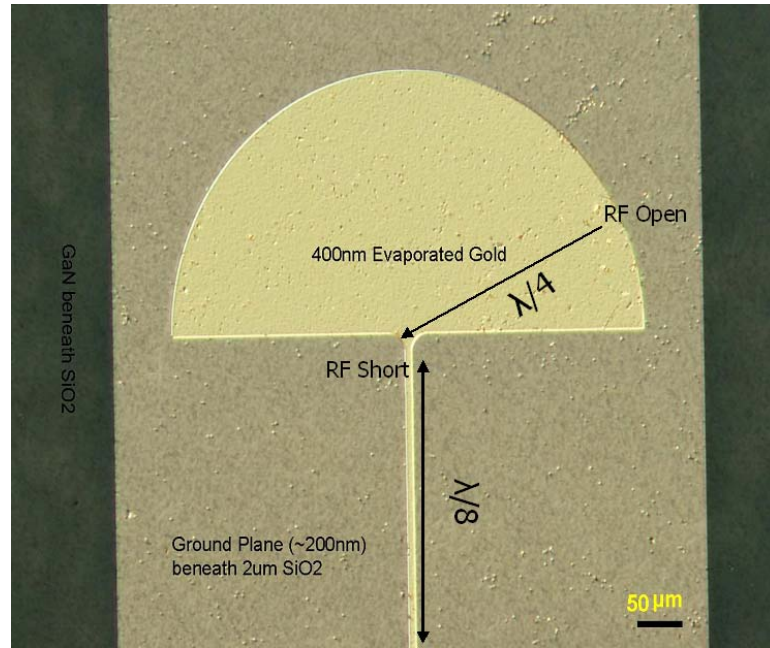


Figure 2.24: Optical microscope photograph of a fabricated resonator.

### 2.2.5.2 Small-Signal Microwave Characterization

One port S-parameter measurements of the diodes were performed and processed to de-embed the parasitics and extract the active region impedance. The procedure rests on the equivalent circuit assumption shown in Figure 2.25.

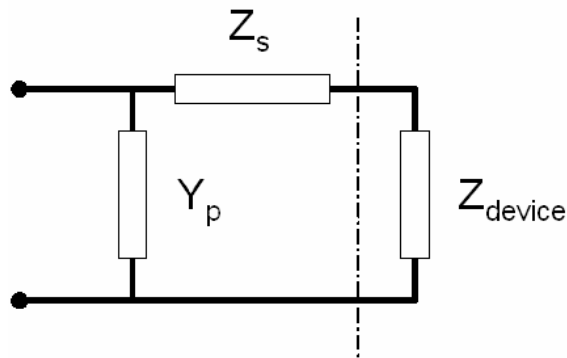


Figure 2.25: Equivalent circuit used to extract the impedance of the active region.

On the chip, adjacent to the real device, we also fabricated a shorted and open version of the device for RF characterization purposes. Shorted version is simply the



diagnostic device which does not have the active mesa compared to the real diode. Open version is defined by preventing electrical contact during the air-bridging. Measured s-parameters from these three structures (Figure 2.26) allow us to uniquely extract the active mesa impedance through S matrix transformations.

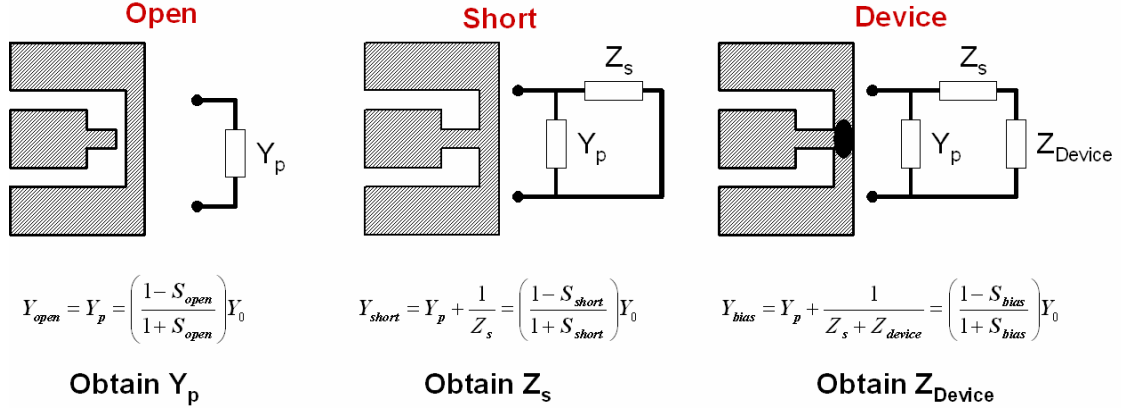
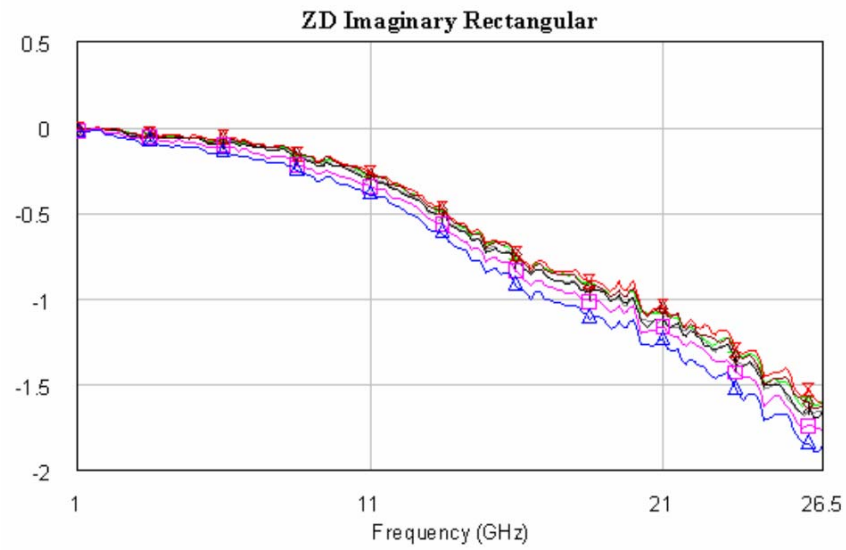
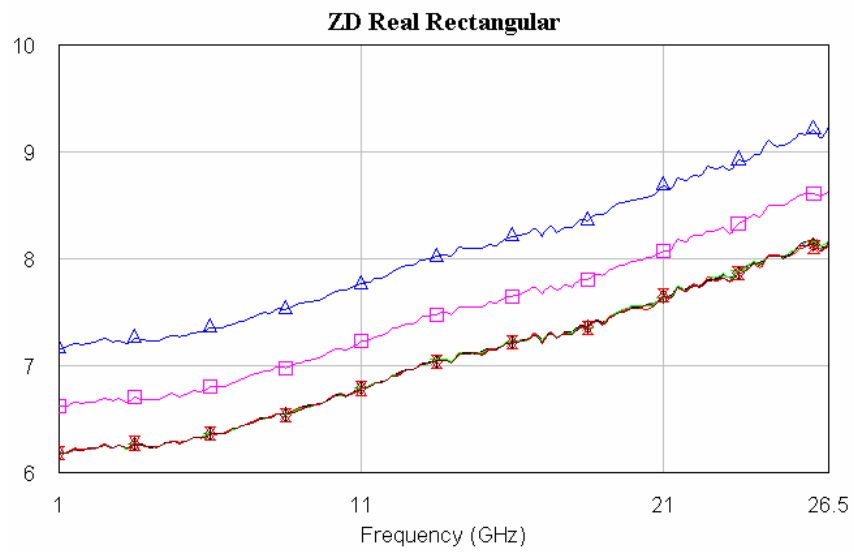


Figure 2.26: Diagram showing the procedure for device impedance extraction.

The s-parameter measurements are transferred to the computing platform in the form of s2p files and the subsequent calculations have been programmed and performed in Matlab. The small signal characterization was performed using Agilent 4142B modular DC source, 8510C Network Analyzer and a 5515A S-parameter test set. The measurements were performed and recorded through ICCAP software. On wafer one-port LRM calibration was used to calibrate the network analyzer for the standards.



(a)



(b)

Figure 2.27: (a) Reactive and (b) resistive part of the impedance as a function of bias. Measured on a 5  $\mu\text{m}$  device. Triangle is zero bias. Vertical axis is in ohms.

Figure 2.27 shows the real and imaginary parts of this extracted impedance. It is observed that the real part is also a function of the frequency (as expected) and increases with increasing frequency.

Table 2-7: RF model for 5  $\mu\text{m}$  diode.

Bias	Parameter	Value
0.5 V	$L = 9 \text{ pH}$	$R=3.35 \text{ } \Omega$
1 V	$L = 8.3 \text{ pH}$	$R=3.5 \text{ } \Omega$

Table 2-8: RF model for 10  $\mu\text{m}$  diode.

Bias	Parameter	Value
0.5 V	$L = 6.5 \text{ pH}$	$R=0.87 \text{ } \Omega$
1 V	$L = 2.65 \text{ pH}$	$R=0.98 \text{ } \Omega$
2 V	$L = 1.7 \text{ pH}$	$R=1.14 \text{ } \Omega$

It is puzzling to see that the reactive part behaves like a negative inductor (reactance increases with increasing frequency). One possible cause could be the extreme magnetic field around the mesa due to the enormous current flowing. Table 2-8 show the inductance and resistance values extracted as a function of bias. For both 5  $\mu\text{m}$  and 10  $\mu\text{m}$  diameter diodes, the inductance is observed to decrease consistently. On the other hand the resistive part did not display much variation. Also, larger diameter diodes seem to exhibit less inductance. It should be noted that these could very well be artifacts due to the diode impedance extraction procedure we employed and also quality of the network analyzer calibration. We have ignored these results and continued to assume that the diode is capacitive and needs an inductive termination for resonance.

## 2.3 Thermal Simulations

The thermodynamic problem of calculating the steady-state channel temperature as a function of dc power dissipation and device dimensions is important from the perspective of gaining more intuition into understanding the operating limits of these devices. Below, the analytical treatment of the problem is presented with respect to the geometry shown in Figure 2.28. This treatment is very intuitive indeed since the results turn out to be products of exponents representing each region and the thermal ground temperature also appears as a multiplying factor in this product.

### 2.3.1 Perpendicular Flow - Region 1 - With thermal generation

Fourier Heat Conduction law states that, gradient of temperature at a point in space is always proportional to the power current density ( $W/cm^2$ ) passing through that point. *In other words, power current follows the direction of maximum temperature drop.*

$$\sigma_{GaN}(T) \frac{dT}{dx} = -P \quad (2.26)$$

where  $P$  is in units of  $W/cm^2$ . In addition, law of thermodynamics also states;

$$Q = \lambda m T \quad (2.27)$$

Where  $Q$  is the *heat energy* in Joules, and  $\lambda$  is the specific heat in units of *Joule/(gr  $\times$  K)* and  $m$  is the mass and  $T$  is temperature in Kelvin.

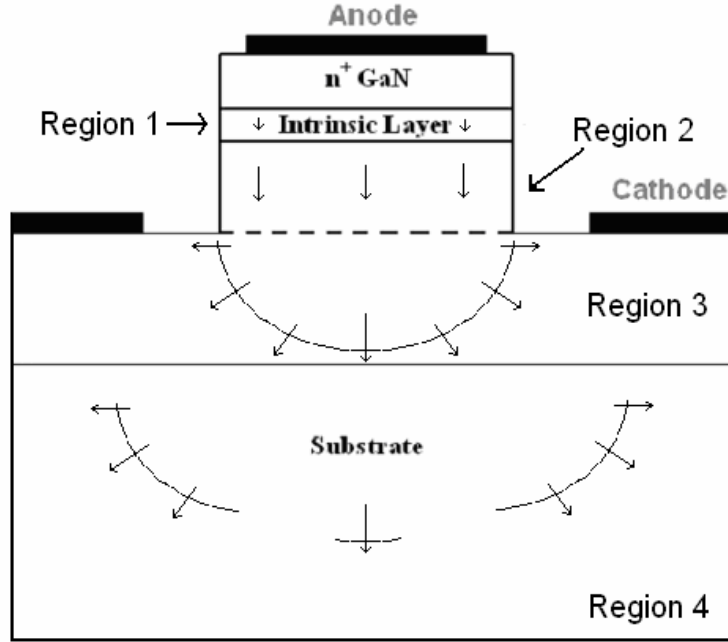


Figure 2.28: Cross-sectional geometry used in analytical thermal calculations.

Now, as can be seen from the figure, perpendicular flow of energy is assumed, with every increment in the positive  $x$  direction, power current increases since each infinitesimal plane generates power and integration needs to be done. Therefore we have;

$$\left. \frac{dT}{dx} \right|_{x=x_1} = -\frac{Qx_1}{\sigma(T)} \quad (2.28)$$

This assumes that thermal energy is not being consumed by any other mechanism so that the power current is continuous. Now if we assume the validity of a highly accepted model;

$$\sigma_{GaN}(T) = \frac{\sigma_{GaN}^{300K} \times 300K}{T} = \frac{K_{GaN}}{T} \quad (2.29)$$

The solution of (2.26) is given by;

$$\frac{1}{T} \frac{dT}{dx} = -\frac{Qx}{K_{GaN}} \quad (2.30)$$

### 2.3.2 Perpendicular Flow - Region 2 - Without thermal generation

When there is no generation, the equation is;

$$\frac{dT}{dx} = -\frac{P}{\sigma_{GaN}(T)} \quad (2.31)$$

where  $P$  is in units of  $W/cm^2$  and it represents the total power current coming down in the parallel flow region.

Now if we use the temperature dependence, we have;

$$\frac{1}{T} \frac{dT}{dx} = -\frac{P}{K_{GaN}} \quad (2.32)$$

and,

$$\ln[T(x)] \Big|_{x=0}^{x=\delta} = \ln[T(\delta)] - \ln[T(0)] = -\frac{P\delta}{K_{GaN}} \quad (2.33)$$

Thus,

$$T(\delta) = T(0) \exp \left[ -\frac{P\delta}{K_{GaN}} \right] \quad (2.34)$$

Here  $P$  is the power per  $cm^2$ ,  $\delta$  is the approximate distance which heat travels in the perpendicular direction. This is taken to be roughly 80% of the ‘half’ of the smaller radius. The more detailed case of electron contribution to the heat conduction Appendix 1.

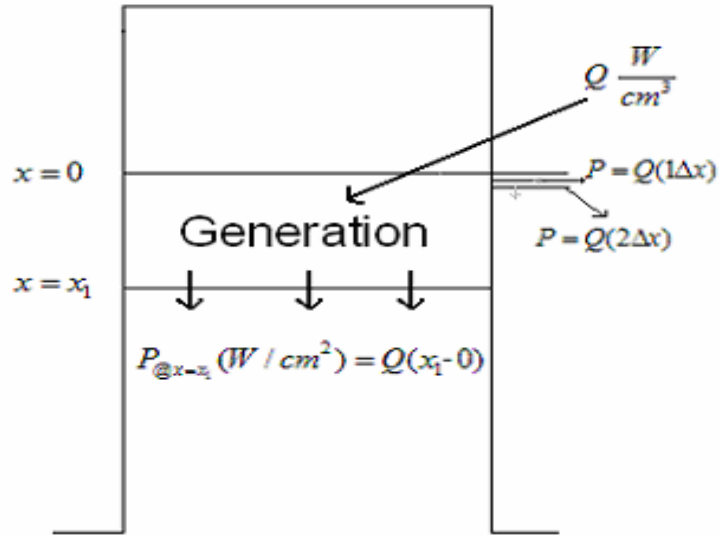


Figure 2.29: Diagram showing how the equations were set-up.

The assumption is this: Top-most Region, below the contact is assumed to be the highest temperature point in these calculations, therefore heat always, in steady-state flows in the downward direction.

Now if the situation is as described in figure two, then in the region where power is being generated, the equation to solve is;

$$\left. \frac{dT}{dx} \right|_{x=x_1} = -\frac{Qx_1 + P}{\sigma(T)} \quad (2.35)$$

### 2.3.3 Spherical heat flow under the mesa - Region 3

The same equation in the previous section becomes (2.36) when spherical spread is integrated into it.

$$dT = -\frac{1}{\sigma_{GaN}(T)} \frac{P \left( \frac{\text{Watts}}{\text{cm}^2} \right) \times w \times L}{\frac{1}{2} (2\pi r) \times L} dr = -\frac{1}{\sigma_{GaN}(T)} \frac{wP}{(\pi r)} dr \quad (2.36)$$

Thus, assuming the same temp dependence.

$$\frac{1}{T} \frac{dT}{dr} = -\frac{wP}{\pi K_{GaN}} \frac{1}{r} \quad (2.37)$$

Integrating both sides,

$$\ln \left[ \frac{T(r_2)}{T(r_1)} \right] = -\frac{wP}{\pi K_{GaN}} \ln \frac{r_2}{r_1} \quad (2.38)$$

And

$$T(r_2) = T(r_1) \exp \left[ -\frac{wP}{\pi K_{GaN}} \ln \frac{r_2}{r_1} \right] \quad (2.39)$$

#### 2.3.4 Spherical heat flow through SiC Substrate - Region 4

With respect to the given geometry, this component is given by;

$$T(r_3) = T(r_2) \exp \left[ -\frac{wP}{\pi K_{SiC}} \ln \frac{r_3}{r_2} \right] \quad (2.40)$$

$T(r_3)$  is assumed to be thermal ground. Therefore, the temperature right beneath the mesa,  $T(0)$  is;

$$T(0) = T(\delta) \exp \left[ \frac{P\delta}{K_{GaN}} \right] \quad (2.41)$$

$$T(\delta) = T(r_1) = T(r_2) \exp \left[ \frac{wP}{\pi K_{GaN}} \ln \frac{r_2}{r_1} \right] \quad (2.42)$$



$$T(r_2) = T(r_3) \exp \left[ \frac{wP}{\pi K_{SiC}} \ln \frac{r_3}{r_2} \right]$$

Therefore, combining all of these results.

$$T(0) = T(r_3) \exp \left[ \frac{wP}{\pi K_{SiC}} \ln \frac{r_3}{r_2} \right] \exp \left[ \frac{wP}{\pi K_{GaN}} \ln \frac{r_2}{r_1} \right] \exp \left[ \frac{P\delta}{K_{GaN}} \right] \quad (2.43)$$

$T(r_3)$  in this context is the thermal ground and be assumed 300 °C or a little less.

Equation (2.43) can be plotted in various ways. For instance, first one can look at the channel temperature vs. current density as plotted in Figure 2.30. This plot assumes 1 MV/cm<sup>2</sup> in the  $P = E.J$  variable. Two values for GaN thermal conductivity has been compared in this figure and it shows that imperfections (thermal boundary resistivities) which may be interpreted as a reduction in the over all thermal conductivity of the GaN material from 2.0 W/cm-K to 1.5 W/cm-K can cause a channel temperature increase of ~150 °C. This is an important insight since the effect of thermal boundary conditions have been experimentally shown in HEMTs by Kubal et al. to be significant. As a result of this, GaN on GaN HEMT operation runs cooler than both GaN on diamond and GaN on SiC.

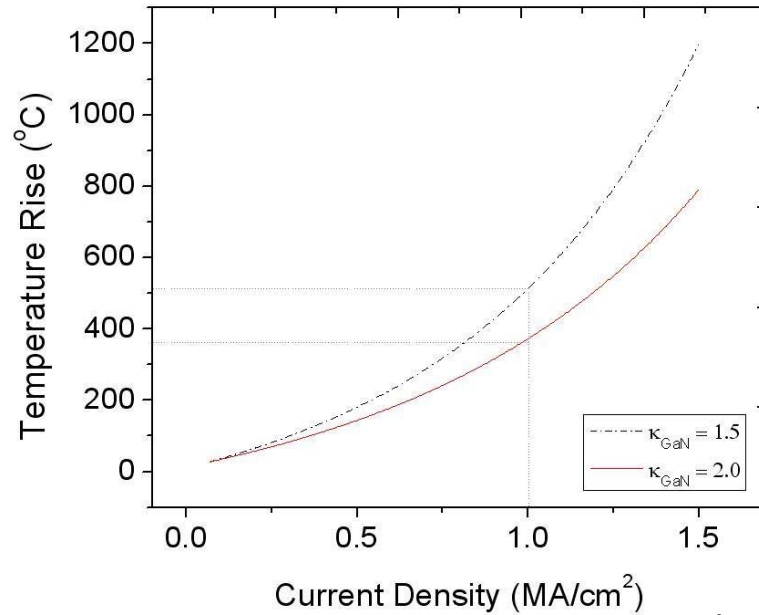


Figure 2.30: Channel temperature vs. Current density.  $E = 1 \text{ MV/cm}^2$ .  $\kappa_{\text{SiC}} = 3 \text{ W/cm-K}$ . Thermal Ground =  $300^\circ\text{K}$ . SiC Thickness =  $250 \mu\text{m}$ , Cathode Level  $n^{++}$  Thickness =  $700 \text{ nm}$ .

Another useful plot would be to fix every other variable and plot the channel temperature as a function of the diode diameter. This is shown in Figure 2.31 for two different substrates showing tremendous benefit available from using a SiC substrate with its superior thermal conductivity.

In Figure 2.32 below, channel temperature vs.  $w$  is plotted for a wall-type device for two different channel lengths. This plot clearly shows that the returns are diminishing beyond  $10 \text{ nm}$  width. Anyway at this dimension, surface depletion would raise a serious limitation let alone the tremendous fabrication challenge it presents.

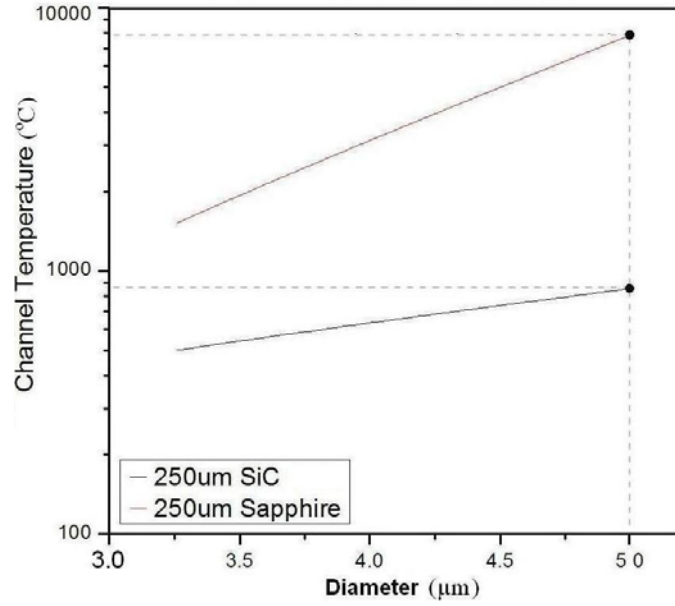


Figure 2.31: Channel temperature vs Diameter simulations.  $J=0.65 \text{ MA/cm}^2$ ,  $E = 1\text{MV/cm}^2$ . GaN epilayer thickness  $1.2 \text{ μm}$ .  $\kappa_{\text{GaN}}=2 \text{ W/cm-K}$ ,  $\kappa_{\text{SiC}}=3 \text{ W/cm-K}$ . Thermal Ground =  $300 \text{ °K}$ . Parameters are chosen after sample GS2341.

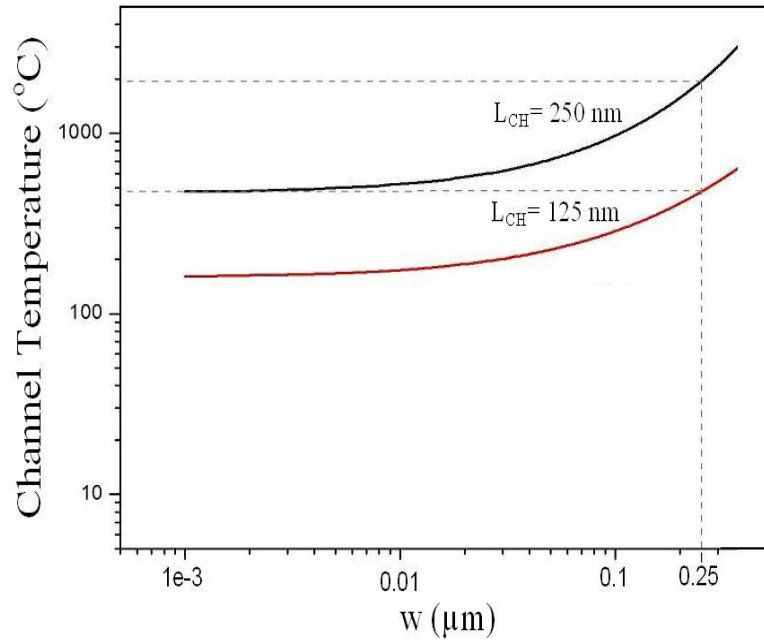


Figure 2.32: Channel temperature vs.  $w \text{ (μm)}$  for 125 and 250 nm long (vertical) ballistic region.  $J = 1 \text{ MA/cm}^2$ ,  $E = 500 \text{ kV/cm}^2$ .  $\kappa_{\text{GaN}}=2 \text{ W/cm-K}$ ,  $\kappa_{\text{SiC}}=3 \text{ W/cm-K}$ . Thermal Ground =  $300 \text{ °K}$ . SiC Thickness =  $250 \text{ μm}$ , Cathode Level  $n^{++}$  Thickness =  $700 \text{ nm}$ .

### **2.3.5 Conclusion**

In the light of these simulations, it has been shown that feasible operating channel temperatures are possible only with extremely narrow wall type devices. This is the only geometry which is capable of draining the excessive thermal energy arising due to extreme current density and electric field required by device operation.

To achieve these feasible channel temperatures with cylindrical geometry, the device diameter needs to be reduced to impractical values which will present nearly impossible impedance matching problems. This situation can easily be fixed for wall type devices by making them as long as necessary to achieve the required mesa surface area. Therefore our conclusion is that this research can advance only with further investigations on the wall type devices and abandoning the cylindrical diodes. Wall type devices can also be thought as many small cylindrical devices in parallel connection.

## CHAPTER 3

# Negative Effective Mass Vertical Diode Processing

### 3.1 Introduction

A very large part of this thesis research effort was spent in process development for the fabrication of different diode structures. Discussions in this chapter will detail the process steps involving vertical device structures designed to implement the band diagram discussed in the previous section.

### 3.2 Vertical Cylindrical Mesa Process

The diode cross-section is shown in Figure 3.1. The wafers were grown in a GEN2 molecular beam epitaxy system (MBE) by Xiaodong Chen. The growth sequence is (top to bottom) is as follows:

- $n^{++}$  GaN for the anode contact.
- Intrinsic GaN layer for ballistic injection.
- 20%  $n^{++}$  AlGaN
- $n^{++}$  GaN for cathode contact
- AlN buffer (which serves for nucleation and preparation of Sapphire surface for GaN growth)

Two different processes have been developed to fabricate these devices: (i) Air-Bridge Process (ii) Dielectric-Bridge Process. These are merely two different means of establish an electrical contact to the diode from the much larger contact pads for on-

wafer electrical characterization. These pads are sized for 150  $\mu\text{m}$  or 250  $\mu\text{m}$  pitch cascade probes (Ground-Signal-Ground). Air-Bridge Devices

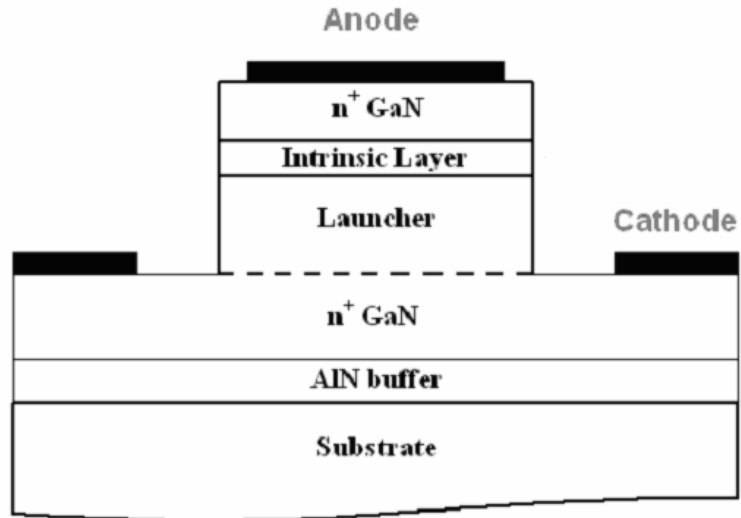


Figure 3.1: Cross-sectional view of the cylindrical diode structure

### 3.2.1.1 Alignment Marks

For proper and accurate lithographic overlay, it is necessary to deposit metal alignment marks as the first thing in the process. In practice, for the placement of the alignment marks, either of e-beam lithography or photolithography can be used (given the mask is fabricated accurately). However; in general, e-beam lithography is more popular due to better resist edge acuity and accurate feature placement. For small chips, the exposure time cost is usually not more than the total photolithographic process. In the beginning of the process run, a thorough solvent cleaning procedure is applied with acetone, methanol and isopropyl alcohol (IPA), preferably in ultrasonic bath. Next, samples are spin coated with a bi-layer stack of P(MAA-MMA)/PMMA (e-beam lithography resist) for lift-off and baked at 170  $^{\circ}\text{C}$  for 15 minutes following each spin coating. Bi-layer stack is preferable as co-polymer (P(MAA-MMA)) develops faster than PMMA for the same dose in MIBK:IPA(1:1) developer. This

gives the stack a natural undercut profile. To prevent charging (which causes coulomb deflection of the electron beam) during lithography, EZ Spacer is spin coated to form a thin conductive layer and baked at 150 °C for 1.5 minutes right after the bi-layer stack. For finer lithographic requirements, one can sputter gold atop the resist. EZ Spacer is easily removed by DI water rinsing right after exposure and before development.

Next, a stack of titanium (15 nm) and platinum (125 nm) is evaporated in vacuum and lifted-off (overnight) in methylene chloride. Platinum is chosen since: (i) it can withstand high temperatures up to 850 °C and thus, won't deform and lose edge acuity during the ohmic anneal process and (ii) it is a high-Z metal making it suitable for proper detection by the electron beam alignment system.

### **3.2.1.2 Mesa Etch**

Various diameters of cylindrical mesas are created using dry etch techniques (Figure 3.4a). Photolithography is chosen for mesa definition and GCA 200 Autostepper is used with 5 inch masks fabricated using Heidelberg Laser Writer. Following a 90 °C hard-bake to harden the photoresist, Plasma Therm 770 ICP-RIE system is used for etching GaN in a chlorine based chemistry (Figure 3.4b).

In this chemistry, inert Argon creates the plasma,  $\text{BCl}_3$  provides the heavy mass ions for physical bombardment to break the crystal bonds on the surface. Chlorine species chemically attracts and removes the material. Low chamber pressure (6 mTorr) is used to achieve a longer mean free path allowing ions to build more kinetic energy. There is a good body of literature on this subject [23 - 26]. There are a number of trade-offs pertaining to etching parameters. One can adjust and optimize the gas flow rates,

power levels and gas pressure to achieve a particular etch rate with varying degrees of verticality and smoothness. Table 3-1 summarizes the process details for this dry etch step.

Table 3-1: GaN mesa etch ICP recipe

PARAMETER	VALUE
Pressure	6 mTorr
ICP Power	350 Watts
RIE Power	35 Watts
Ar	6 sccm
Cl <sub>2</sub>	8 sccm
BCl <sub>3</sub>	17 sccm
DC Bias (typical)	98 Volt
GaN Etch Rate	104 nm/min
1813 Shipley	189 nm/min
Carbon	15 nm/min

Table 3-2: Mesa Etch Process (air-bridge devices)

Step	Parameter
Sample Cleaning	<ul style="list-style-type: none"> <li>Acetone, IPA rinse, N<sub>2</sub> blow-dry.</li> <li>DI water rinse, N<sub>2</sub> blow-dry</li> <li>115 °C de-hydration bake on hotplate, 3 minutes.</li> </ul>
Resist Coating	<ul style="list-style-type: none"> <li>P20 Primer spun for 30 sec at 3000 rpm.</li> <li>SPR 955 CM-0.9, spun for 30 sec at 3000 rpm.</li> <li>Soft-bake at 90 °C, for 2 minutes.</li> </ul>
Exposure	<ul style="list-style-type: none"> <li>GCA 200 Autostepper, f=0, Time = 0.3 sec.</li> </ul>
Develop	<ul style="list-style-type: none"> <li>MIF 300 for 1min, DI Water rinse, N<sub>2</sub> blow dry</li> </ul>
Descum	<ul style="list-style-type: none"> <li>GLEN 1000 plasma Asher. O<sub>2</sub> plasma descum at 100 Watts. Process #3 for 2 minutes.</li> </ul>
Mesa Etch	<ul style="list-style-type: none"> <li>Plasma Therm 770 ICP Dry Etch.</li> </ul>
Profiling	<ul style="list-style-type: none"> <li>Tencor P10 Profilometer Measurements.</li> </ul>
Resist Strip	<ul style="list-style-type: none"> <li>1165 immersion overnight.</li> <li>Acetones, IPA rinse, N<sub>2</sub> blow-dry.</li> <li>GLEN 1000 plasma Asher. Resist Strip with Process #9 (400 Watts) for 2 minutes</li> </ul>

### 3.2.1.3 Ohmic Contacts

Next step is ohmic contact deposition to form the anode and cathode electrodes.

Anode electrode, by design, is the contact to the top n<sup>++</sup> layer (Figure 3.1). Ohmic



contacts to these diode structures are particularly important due to enormously large current densities resulting from device operation. Poor contacts drop most of the applied bias voltage and significantly reduce the electric field strength in the ballistic region. Comparative experimental studies of various ohmic contact metallization schemes have been performed and the results will be discussed in CHAPTER 6

Table 3-3: Ohmic Contact Deposition

Step	Parameter
Sample Cleaning	<ul style="list-style-type: none"> <li>▪ Acetone, IPA rinse, N<sub>2</sub> blow dry.</li> <li>▪ DI water rinse, N<sub>2</sub> blow dry</li> <li>▪ 15 °C de-hydration bake on hotplate, 3 minutes.</li> </ul>
Resist Coating	<ul style="list-style-type: none"> <li>▪ LOR 5A, spun for 30 sec at 3000 rpm.</li> <li>▪ Soft-bake at 180 °C for 5 minutes.</li> <li>▪ SPR 955 CM-0.9, spun for 30 sec at 3000 rpm.</li> <li>▪ Soft-bake at 90 °C, for 2 minutes.</li> </ul>
Exposure	<ul style="list-style-type: none"> <li>▪ GCA 200 Autostepper, f=0, Time = 0.3 sec.</li> </ul>
Developing	<ul style="list-style-type: none"> <li>▪ MIF 300 for 1min, DI Water rinse, N<sub>2</sub> blow dry</li> </ul>
Descum	<ul style="list-style-type: none"> <li>▪ GLEN 1000 plasma Asher. O<sub>2</sub> plasma descum at 100 Watts. Process #3 for 2 minutes.</li> </ul>
Native Oxide Cleaning	<ul style="list-style-type: none"> <li>▪ BOE (30:1) for 30 sec, DI water rinse, N<sub>2</sub> blow dry</li> </ul>
Metal Evaporation	<ul style="list-style-type: none"> <li>▪ CVC 4500 e-gun and Thermal evaporation at 2e-6 Torr pressure.</li> </ul>
Lift-Off	<ul style="list-style-type: none"> <li>▪ 1165 immersion overnight.</li> </ul>
Residual Resist Cleaning	<ul style="list-style-type: none"> <li>▪ Acetone, IPA rinse, N<sub>2</sub> blow-dry.</li> <li>▪ GLEN 1000 plasma Asher. Resist Strip with Process #9 (400 Watts) for 2 minutes.</li> </ul>

Ohmic contact deposition, in theory, can be done in a single lift-off process, as illustrated in Figure 3.4d, e and f. However; experience shows that the resulting bi-layer resist profile (for a ~1 µm gap between the mesa and lower contact) is not mechanically/thermally stable at typical substrate temperatures reached during the evaporation. This prevents a successful lift-off. As a result, the practice of depositing each contact separately has been adapted. Metal pads, delineated by photolithography, are put down along with the cathode level ohmic contacts to reduce fabrication cost.

Ti(15 nm)/Al(90 nm)/Mo(45 nm)/Au(55 nm) composite metal stack is used and annealed at 800 °C following lift-off. In this stack Ti, Al and Mo are evaporated using e-gun, while gold is put down using thermal evaporation.

Along with the devices, rectangular (or circular) TLM (transmission line model) test patterns are also fabricated on the same chip, distributed evenly in the active area (5 to 10 locations) to characterize and get a statistical sense of ohmic contact parameter variations. These extracted parameters are specific contact resistance  $r_c$  ( $\Omega\text{-cm}^2$ ), sheet resistance  $R_{SH}$  ( $\Omega/\square$ ) and the transfer length ( $\mu\text{m}$ ).

Rectangular TLM (transmission line method) test patterns consist of a rectangular mesa etched all the way down to the substrate for isolation (to confine the current into perpendicular flow between the pads) with incremented gap spacing to measure and record the total resistance of the gap as a function its spacing. These TLM test patterns are sized for certain approximations to be valid which allow accurate parameter extraction from these measurements. In our process, a single pad size is  $100\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$  and gap spacing between them spans 5 to  $35\text{ }\mu\text{m}$  with  $5\text{ }\mu\text{m}$  increments.

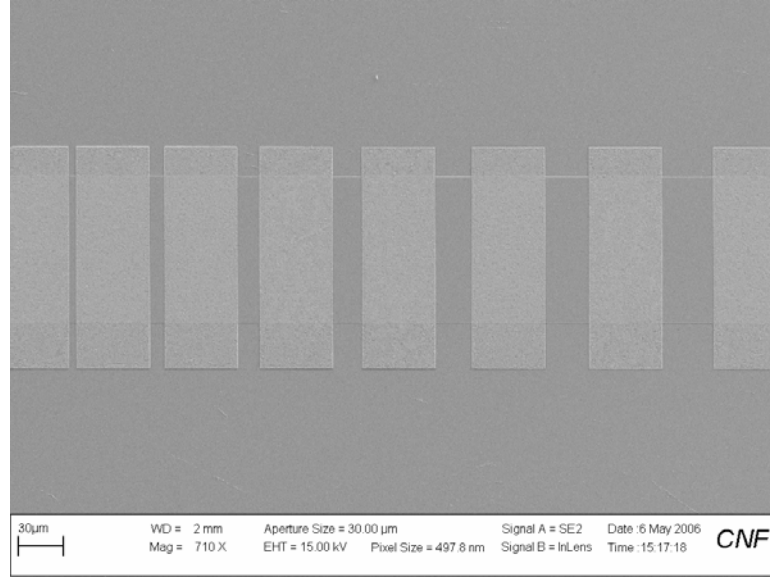


Figure 3.2: SEM image showing a TLM pattern. Electrode separation goes from 5  $\mu\text{m}$  to 35  $\mu\text{m}$  with 5  $\mu\text{m}$  increments.

Following the annealing process, all of these test patterns on the chip are measured and recorded using a four-point-probe station housed in the clean-room. Four-point probe measurements serve the purpose of eliminating all the undesired parasitic loading caused by the cables and other factors. TLM method is reasonably accurate down to  $10^{-7} \Omega\text{-cm}^2$  and parameter extraction process will be detailed in CHAPTER 6.

#### 3.2.1.4 Device Isolation Etch

An etch step in order to electrically isolate individual devices is required right after the ohmic contacts are put down. During this step, GaN epilayers (except for the device area) is completely etched down all the way to the substrate level to prevent all current conduction between the electrodes. This etch step is performed after the ohmic contact deposition deliberately in order to minimize prior processing of this area, thus contamination, which degrades ohmic contact. The same ICP recipe that was used to

etch the mesas can be used with increased ICP power (450 Watts instead of 350 Watts) in order to reduce the etch time since the etch is deeper.

### **3.2.1.5 Air-Bridging**

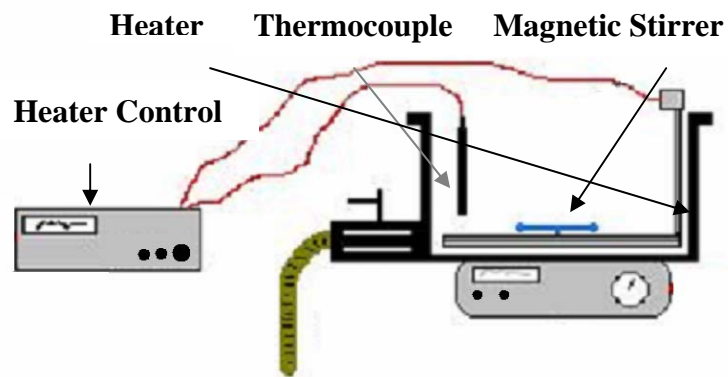
Electrical connection between the anode electrode of few microns size and the hundreds of microns size probe pads is accomplished by the fabrication of an air-bridge. This process step begins by defining the position of the bridge legs using photolithography (Figure 3.4g). One of the legs needs to coincide with the top of the mesa (the anode electrode) and the other needs to land on the edge of the signal (center) pad. A relatively thicker photoresist (i.e. Shipley 1827, spins  $\sim 2.7\mu\text{m}$  thick) is chosen to create the *mold* for this step to achieve higher electrical current and thermal current conduction capacity. The resulting photoresist openings after the exposure is intentionally made smaller than that of the anode and centered on the contact to leave margin for misalignment. However; this is not illustrated in Figure 3.4g.

This lithography step is followed by the deposition of the seed layers which serves to conduct the necessary current through the entire exposed surface during the plating process (Figure 3.4h). The seed layer is composed 15 nm of Ti for adhesion, and a thermally evaporated 75 nm Au for conduction. The Au layer is not made any thicker since it will have to be removed with gold etchant later and this will also consume the electroplated gold at the same time. No lithography is necessary for this metallization.

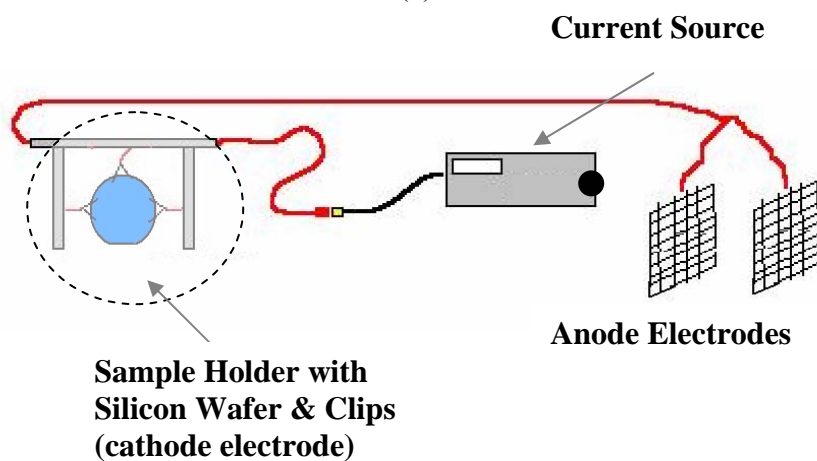
The final step before plating is the creation of the photoresist mold for the bridge itself which will electrically connect the two openings on the previous layer (Figure 3.4i). This exposure must completely open up both leg locations, previously defined by the underlying resist openings, and the path connecting them which will conduct the

current between these two points. Extra care must be exercised during this *second* photoresist spin coating sequence since regular 115 °C hot-plate soft-bake presents the danger of re-flowing the underlying first level resist and as a result damaging the seed layer atop. Our practice has been to soft-bake for 5 minutes at 90 °C for this particular photolithography step. This deviation from the recommended temperature is tolerable since this lithography step is not very demanding in terms of feature size accuracy.

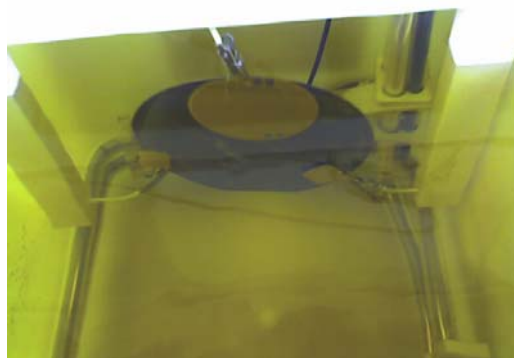
Having completed the plating preparations (Figure 3.4j), the gold electroplating solution (BDT-510) is heated to 50 °C while continually stirred using the magnetic system. Samples need to be carefully attached to the current source clips to ensure current conduction (Figure 3.3c). To accomplish this, photoresist at the corners of the chip can be easily removed by a Q-tip dipped in Acetone. One must be careful though not to have too much Acetone on the Q-tip and to prevent the situation that when pressure is applied, it will spread over a much larger area of lithography than intended and potentially ruin it. Extra care should also be exercised to make sure that the tips of the clips (which have to be in electrical contact with these photoresist free gold exposed corners) are cleaned and rust free so they can conduct current. A P10 step-height measurement is taken after a few minutes of deposition to measure the deposition rate. This measurement was taken at the edges of the metal contact pads since they were large enough to give enough area for the P10 profilometer tip to fit and move freely. The entire electroplating set-up is shown in Figure 3.3a and b. Figure 3.3c shows a photograph taken during the plating.



(a)



(b)



(c)

Figure 3.3: Electroplating set-up (a) Initial set-up showing the tank, stirring and the heating system (b) The electrodes which need to be dipped in the tank filled with solution along with the sample holder. (c) A photograph showing inside the actual set-up.

An important issue to mention here is that the gold deposition rate would be uncontrollably high for current densities in the order of  $\sim 10 \text{ A/cm}^2$ . This situation is naturally created if one draws 100 mA current through a typical exposed chip area of  $\sim 1 \times 10^{-2} \text{ cm}^2$  (10 mm  $\times$  10mm chips). To remedy this situation, we used a set-up which introduces a larger effective electroplating surface using a 4" silicon wafer that was coated with the same seed layer along with the samples.

Table 3-4. Air-Bridge Process for the Vertical Cylindrical Diodes

Step	Parameter
Wafer Clean	▪ Acetone, Methanol, IPA
De-Hydration Bake	▪ 115 °C Hot Plate, 3 min.
Resist Coating	▪ S-1827, 3000 rpm, 30 sec (spins 2.7 $\mu\text{m}$ )
Soft-Bake	▪ 115 °C Hot Plate, 2 min
Exposure	▪ 5X stepper, f=260, t=1.2 sec.
Develop	▪ In 300MIF, 60 sec.
Hard-Bake	▪ 130°C oven, 30 min.
Descum	▪ GLEN 1000 plasma Asher. O <sub>2</sub> plasma descum at 100 Watts. Process #3 for 2 min.
Seed Layer Evaporation	▪ Ti/Au (150A/750A)
Vapor Prime Coating	▪ YES oven, HMDS 34 min
Resist Coating	▪ S-1827, 3000 rpm, 30 sec.
Soft-Bake	▪ 90 °C Hot Plate, 5 min.
Exposure	▪ 5x stepper, f=260, t=1.5 sec.
Develop	▪ 300 MIF, 60 sec.
Descum	▪ GLEN 1000 plasma Asher. O <sub>2</sub> plasma descum at 100 Watts. Process #3 (2 min.)
Plating Setup	▪ BDT-510(250 ml), 55 °C, stirring
Plating	▪ Set J= $\sim 3 \text{ mA/cm}^2$ , 2 m $\sim 1 \text{ m Au}$ /12.5 min.
Flood Exposure	▪ HTG contact aligner, 30 sec.
Develop	▪ 300 MIF, 60 sec.
Au Etch	▪ TFA gold etch, 60 sec.
Ti Etch	▪ BOE (30:1), 2 min.
Resist Strip	▪ 1165 stripper, 20 min.

The fabricated chip is attached to the middle of the silicon wafer through conducting needles (soldered on the gold) so that the electric field lines inside the solution are

uniform over the chip area ensuring more uniform deposition. During the plating process, deposition rate can be continually measured by profiling the large openings in the resist whose step-height will be continually decreasing. After plating, first, the top-most photoresist layer is removed using the 1165 photoresist stripper (Figure 3.4k). This is followed by the removal of the seed layer (except underneath the air-bridge) using gold etchant and BOE 30:1 (for Ti) as shown in Figure 3.4l. This exposes the first layer of photoresist that was used to *mold* the bridge legs, which is again removed by leaving the sample in 1165 overnight. This leads to the final structure shown in Figure 3.4m.

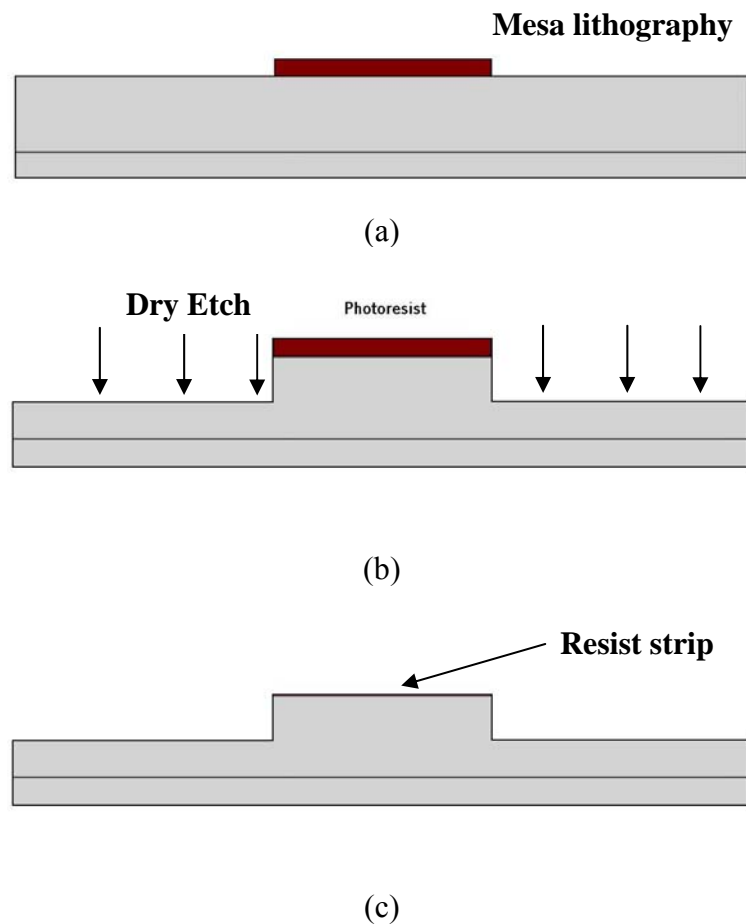
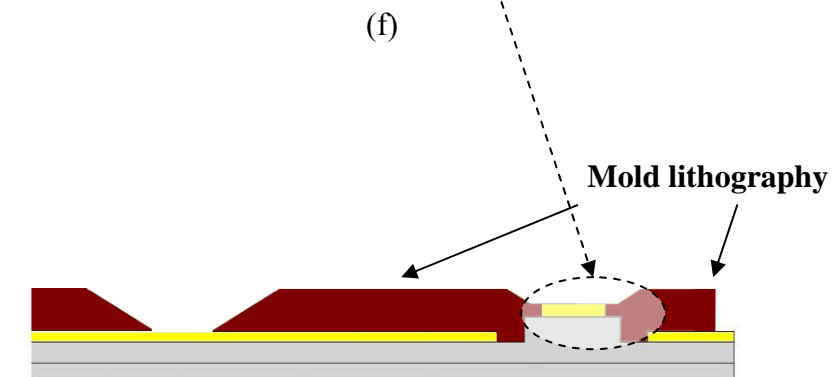
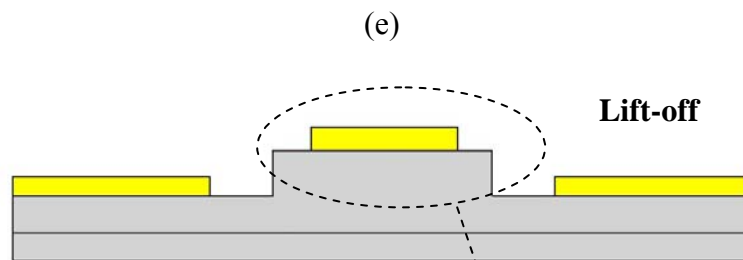
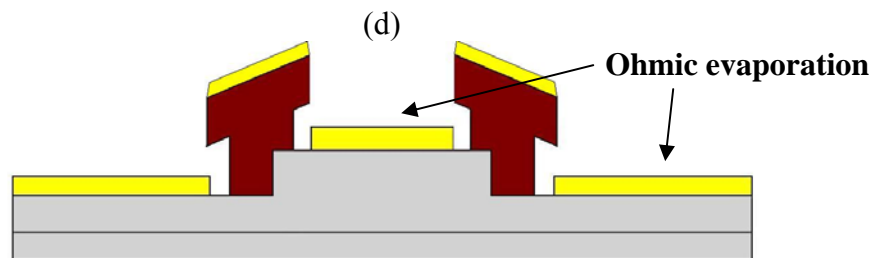
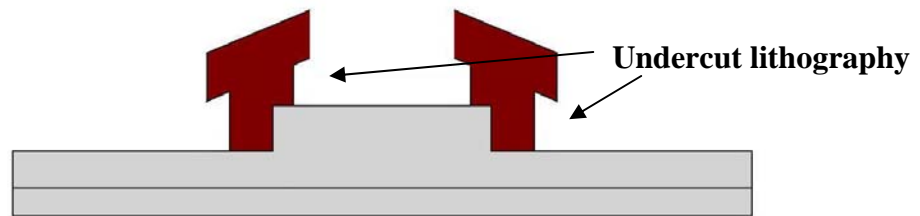


Figure 3.4: Process flow illustration in cross-sectional view

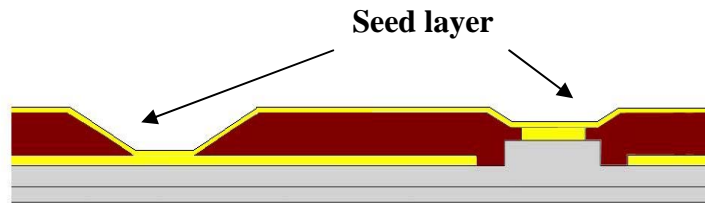


Figure 3.4 continued.

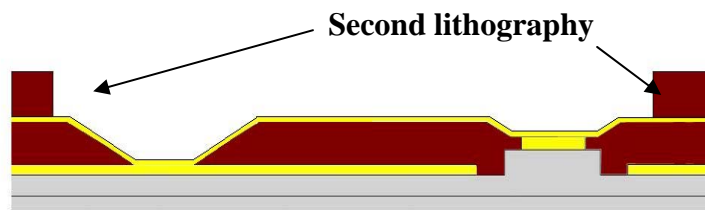


(g)

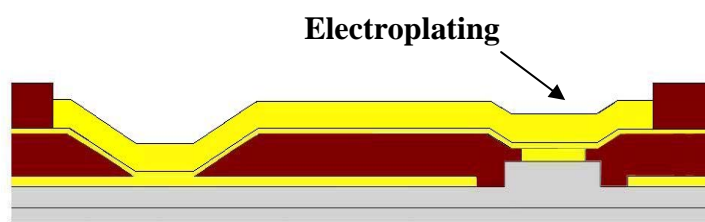
Figure 3.4 continued.



(h)

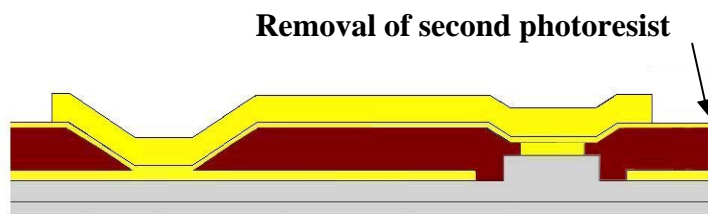


(i)

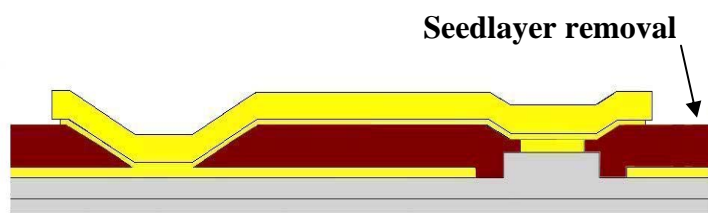


(j)

Figure 3.4 continued.

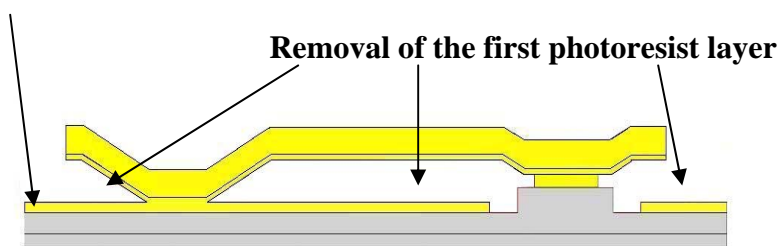


(k)



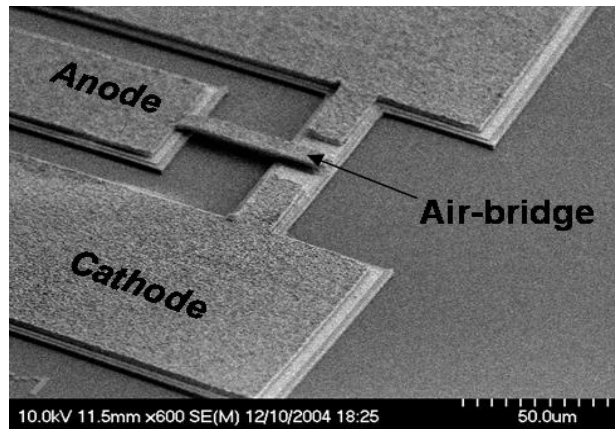
(l)

**Large metal pads**

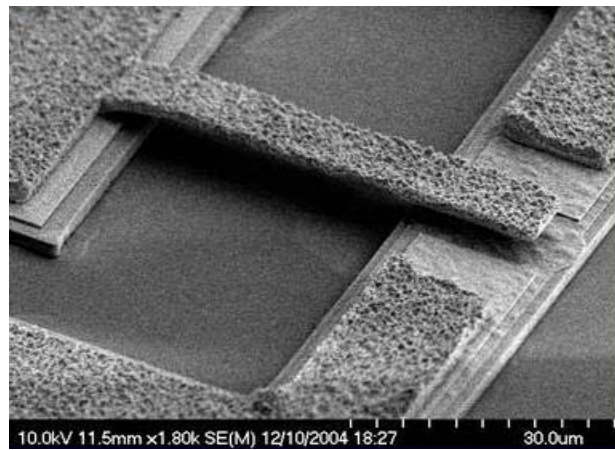


(m)

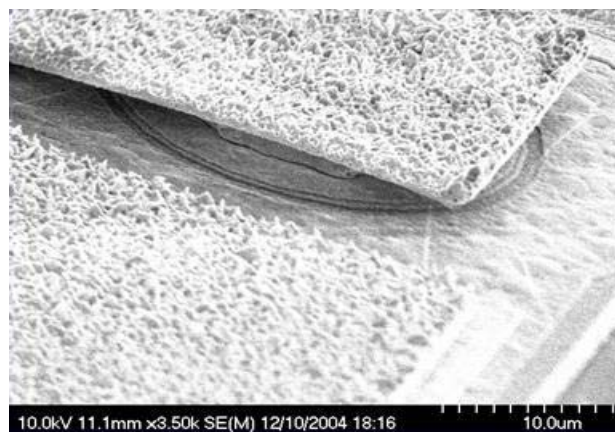
Figure 3.5 shows some SEM images of the fabricated devices using the process described above. Porous nature of the electroplated gold is visible in parts c and d.



(a)



(b)



(c)

Figure 3.5: SEM photographs of fabricated a diode with air-bridge. (a), (b) and (c) are showing various levels of magnifications of the active region. The air bridge is clearly seen suspended in (b).

As mentioned in the previous chapter, most of these devices were eventually destroyed after characterization due to permanent damage they sustained at the ohmic contacts due to extreme joule heating (Figure 3.6).

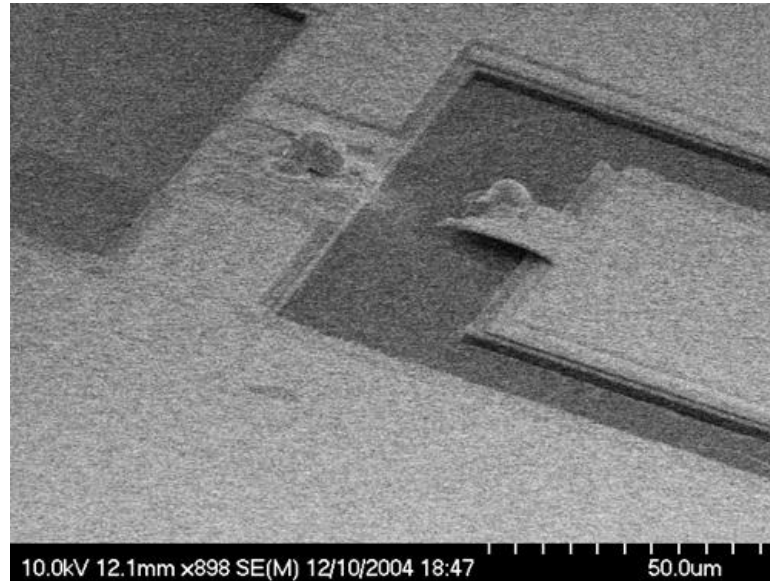


Figure 3.6: Post-Mortem SEM image of a diode with burned air-bridge. Extreme joule heating at the anode contacts permanently destroyed the diodes.

### 3.2.2 Dielectric-Bridge Devices

This approach was developed to enhance heat removal by immersing the active region (where power is dissipated) in a dielectric medium. It also serves the purpose of attaching a planar microwave resonator to the diode. In this approach the plated gold bridge is fabricated on top of dielectric as opposed to suspending in the air.

#### 3.2.2.1 Dielectric Deposition

This process separates from that of the ‘air-bridge’ approach after (device) isolation dry etch. At this point, a  $\sim 2\text{ }\mu\text{m}$  thick amorphous  $\text{SiO}_2$  layer is deposited using the GSI PECVD tool. This thickness ( $2\text{ }\mu\text{m}$ ) is decided based on considerations regarding the

feasibility of metal trace dimensions on the dielectric required by reasonable characteristic impedance values for the microstrip transmission lines. Silicon witness samples were created during the SiO<sub>2</sub> deposition for future characterization.

### **3.2.2.2 Dielectric Etch**

Following the oxide deposition, mesa is uncovered for electrical access. This is accomplished by dry etching the SiO<sub>2</sub> in the Plasma Therm 72 RIE tool. The significant thickness of the SiO<sub>2</sub> layer complicates the achievement of uninterrupted bridge connection and therefore, very small side-wall slope of the oxide opening is required. To accomplish this, the photoresist, delineating the opening, is re-flown in an oven for approximately half an hour after the lithography at ~130 °C. This way, when the dry etch is later performed, the *sloped* photoresist profile is transferred to the SiO<sub>2</sub>. Further decrease in the slope can be achieved by employing an etch recipe with 2:1 (or more) selectivity between photoresist and SiO<sub>2</sub>. However, one has to make sure that the initial photoresist thickness is at least twice that of SiO<sub>2</sub> so that when the desired SiO<sub>2</sub> etch depth is achieved, there is still some photoresist mask is remaining, ensuring the 2 µm SiO<sub>2</sub> everywhere else.

In addition, the removal of residual SiO<sub>2</sub> on the mesa is very important since it will otherwise insulate the electrical contact. Both the deposition and the etch rates have a finite non-uniformity factor over the active chip area (due to small square shape of the sample). This requires that the sloped photoresist opening has to be somewhat smaller than the mesa diameter (0.5 µm works well) since some over etching will be inevitable to make sure the top of all the mesas are opened.

### 3.2.2.3 Contact Pads

Having opened the areas to be electrically contacted, the last step is to put down a thick gold layer (with an underlying Ti layer for adhesion) that will conduct current. The process is identical to the air-bridge step as described above.

## 3.3 Ultra-Narrow Wall Type Mesa Process

Wall type device process was developed primarily to address the excessive joule heating and spreading resistance problems. A rectangular mesa with one side being in the 100 nm – 500 nm range has a tremendous advantage in spreading the resultant thermal energy created within the active mesa. In this design, the mesa is buried in  $\text{Si}_3\text{N}_4$  passivating its sidewalls and creating an efficient thermal contact (with its decent thermal conductivity) maximizing heat removal.

### 3.3.1.1 Mesa Etch

Following the alignment mark lithography (e-beam) and lift-off, an amorphous carbon hard mask is deposited which defines the sub-micron mesa (aspect ratio ranging from  $\sim 1/2$  to 1). Deposition of a reasonably smooth and uniform carbon layer requires experience. Using SC4500 evaporator, stable deposition rate is achieved at 0.5 Å/ sec and  $5 \times 10^{-7}$  Torr chamber pressure. This relatively lower pressure is observed to help prevent *spitting*. In addition, power level needs to be constantly increased in order to maintain this rate and the electron beam occasionally needs to be re-positioned without any sweeping. Direct carbon lift-off attempts were unsuccessful for feature sizes smaller than  $\sim 300$  nm. For such features, the carbon grains were observed to be absent in the resist opening following an SEM characterization. One explanation could be that the relatively larger carbon grains were bouncing off the opening. This has not

been investigated in detail and another approach involving two evaporation steps was adopted to overcome the problem.

Table 3-5. Mesa Etch Process (dielectric-bridge devices)

STEP	PARAMETER
Sample Cleaning	<ul style="list-style-type: none"> <li>▪ Acetone, IPA rinse, N<sub>2</sub> blow dry.</li> <li>▪ DI water rinse, N<sub>2</sub> blow dry</li> <li>▪ 15 °C de-hydration bake on hotplate, 3 minutes.</li> </ul>
Carbon Evaporation	<ul style="list-style-type: none"> <li>▪ CVC 4500 e-gun evaporation at 5e-7 Torr pressure. 0.5 Å/sec deposition rate.</li> </ul>
e-beam resist spin coating	<ul style="list-style-type: none"> <li>▪ % 4 PMMA (495 K) at 3000 rpm for 60 s.</li> <li>▪ % 2 PMMA (950 K) at 3000 rpm for 60 s.</li> <li>▪ EZ spacer at 3000 rpm for 10 s.</li> </ul>
Expose	<ul style="list-style-type: none"> <li>▪ VB6 Leica. 1 nA current, VRU 8.</li> </ul>
Developing	<ul style="list-style-type: none"> <li>▪ Remove EZ spacer by DI rinsing.</li> <li>▪ Develop in MIBK 1:1 for 60 s, DI Water rinse, N<sub>2</sub> blow dry</li> </ul>
Descum	<ul style="list-style-type: none"> <li>▪ GLEN 1000 plasma Asher. O<sub>2</sub> plasma descum at 100 Watts. Process #3 for 2 minutes.</li> </ul>
BOE treatment	<ul style="list-style-type: none"> <li>▪ BOE (30:1) for 30 sec, DI water rinse, N<sub>2</sub> blow dry</li> </ul>
Metal Evaporation	<ul style="list-style-type: none"> <li>▪ CVC 4500 e-gun Chromium evaporation at 2e-6 Torr pressure.</li> </ul>
Lift-Off	<ul style="list-style-type: none"> <li>▪ Overnight lift-off in Methylene Chloride.</li> </ul>
Residual Resist Cleaning	<ul style="list-style-type: none"> <li>▪ Acetone, IPA rinse, N<sub>2</sub> blow-dry.</li> <li>▪ GLEN 1000 plasma Asher. Resist Strip with Process #9 (400 Watts) for 2 minutes.</li> </ul>

In this approach, carbon is first evaporated roughly to a thickness of ~100 nm without any prior lithography. Next, roughly a 10 nm thick chromium mask defining the mesa, alignment marks and other important features are lifted-off atop carbon. Smaller chromium grain size compared to carbon is what permits this lithography and 30 nm thick chromium lift-off has been observed to fail.



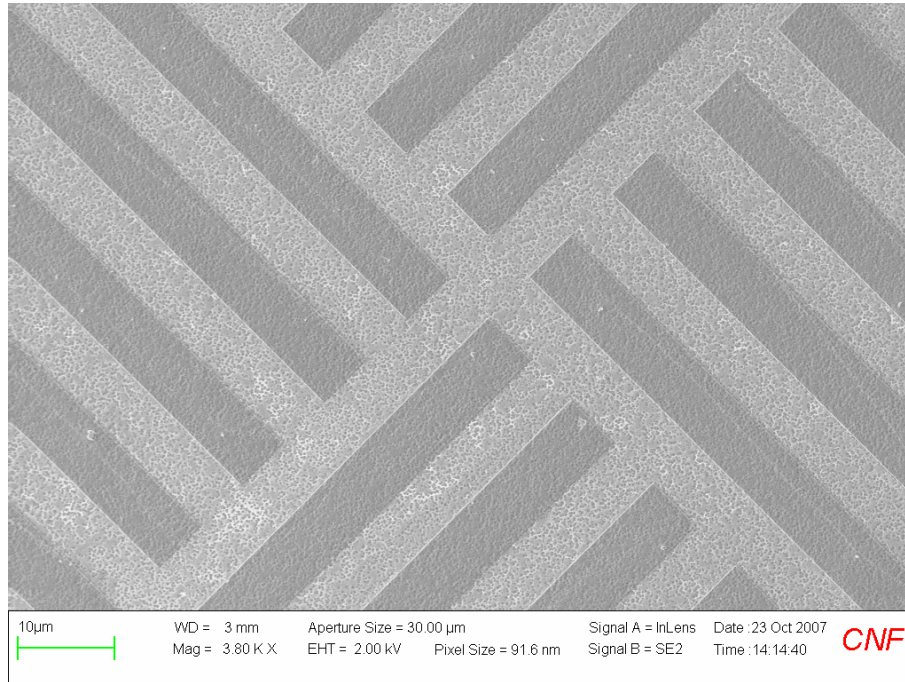
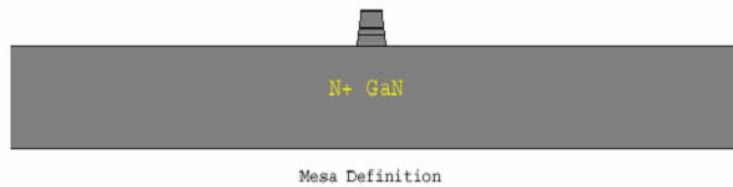


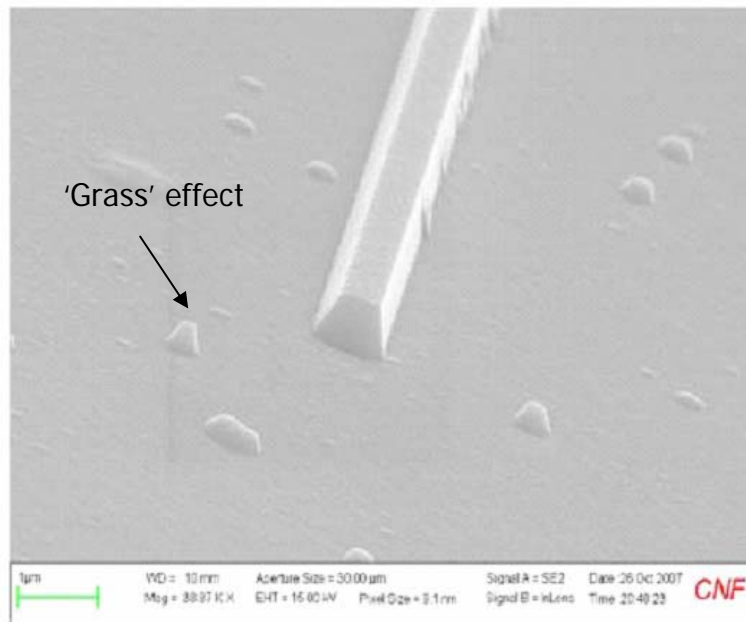
Figure 3.7: Carbon mask patterns - DFAS marks for photolithographic auto-alignment.

Following the chromium lift-off, exposed carbon is ashed in  $O_2$  plasma except in areas masked by chromium. Chromium is then wet etched before the ICP etch, to prevent sputtering and thus potential micro-masking during etch.

Before etching the real samples, the chamber is cleaned using ‘ $O_2$  plasma clean recipe’ to prevent sample contamination. Next, the chamber is conditioned for 15 minutes running the etch recipe without a real wafer inside. This ensures invariant chamber chemistry in the beginning and increases reproducibility of the etch process. During the etching step, a Tencor P10 Profilometer is used to measure etch rates. To be able to accurately monitor the GaN etch, carbon mask consumption rate also needs to be known.



(a)



(b)

Figure 3.8: (a) Cross sectional illustration of the wall type mesa (b) SEM image of a wall type mesa fabricated using carbon mask.. Carbon sputtered during  $O_2$  ashing creates spots of scattered protrusions by masking the material during the etch. Consequent 'Grass' formation is shown in the figure.

Mesa is dry etched using a Plasma Therm 770 Inductively Coupled Plasma (ICP) etching system using chlorine based chemistry with the following parameters:

Table 3-6: Electrical Isolation Etch recipe

Parameters	Value
BCl <sub>3</sub>	17 sccm
Cl <sub>2</sub>	8 sccm
Ar	6 sccm
RF Power 1	35 W
RF Power 2	350W
Pressure	6 mTorr
Average DC Bias	104 V

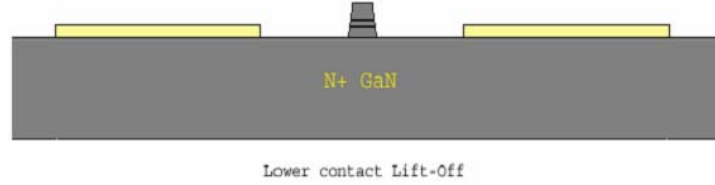
Initial carbon thickness on the sample is measured right before the etching step. In addition, an etch rate estimate is obtained through putting random photolithography on some of the witness samples and etching for a minute or two, then completely removing the photoresist, and profiling the resultant trenches. This rate is measured to be on average  $15\text{nm} \pm 4\text{nm}$  per minute.

Assuming 15 nm per minute carbon loss rate (etch rates are assumed to be time independent but in reality there is a slight time dependence), measured GaN depth is corrected at every P10 measurement. The objective is to etch  $\sim 100\text{nm} \pm 40\text{nm}$  into the lower  $n^{++}$  region to create the plane of the lower level contacts. When the Profilometer measurements (which are corrected for the mask consumption rate) fall within the target, the etch is stopped and the remainder of the carbon mask is ashed in O<sub>2</sub> plasma. At this point, the reader should be aware that O<sub>2</sub> plasma causes some damage to the GaN surface. However, this does not pose as serious a problem as it does in HEMTs and ohmic contacts are not expected to degrade significantly given the  $n^{++}$  doping. Besides, this damage is found to be mitigated by annealing at  $\sim 500^\circ\text{C}$  for 30 seconds

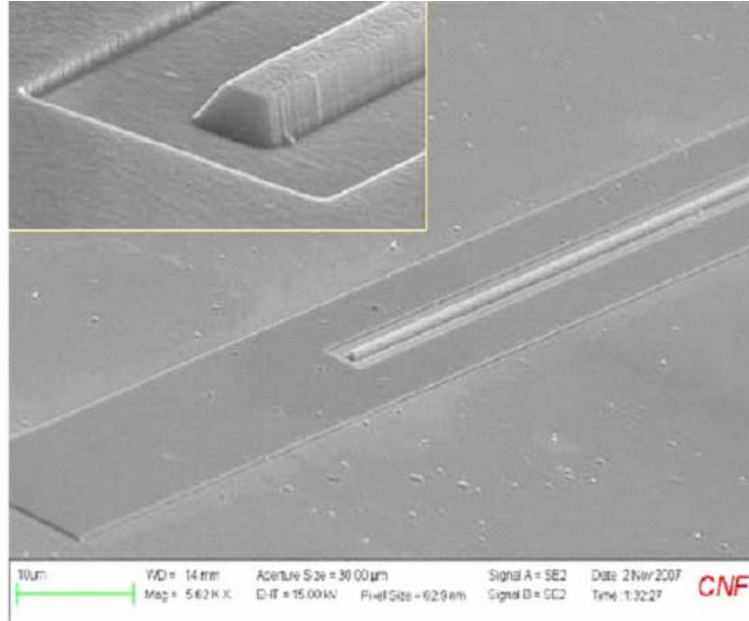
[27] following the removal of the remaining carbon, an average GaN depth of 120 nm is measured confirming the carbon etch rate assumed.

### **3.3.1.2 Ohmic Contacts**

Following the mesa etch step, the cathode contact is delineated using lift-off. However; prior to that, a thorough surface cleaning is performed to ensure optimum conditions for ohmic contact deposition. The cleaning procedure begins with hot (~60-80 °C) trichloroethylene treatment of the sample for an hour to remove any dirt, oil and other contaminants. For some decades, this has been traditionally used as a routine industrial GaAs wafer cleaning procedure before ohmic deposition. Following the bi-layer e-beam resist lithography, routine descum, to etch residual resist and BOE treatment is performed minutes before the metal deposition to remove any undesired native oxide which is detrimental to ohmic contact performance. The metal stack used for the cathode ohmic contact is Ti/al/mo/au system. The sample is then mounted on a chuck and loaded into the evaporation chamber which is immediately pumped down to  $2 \times 10^{-6}$  Torr pressure. Effort was made in the CAD design to minimize the cathode lithography area to save time on the e-beam tool.



(a)

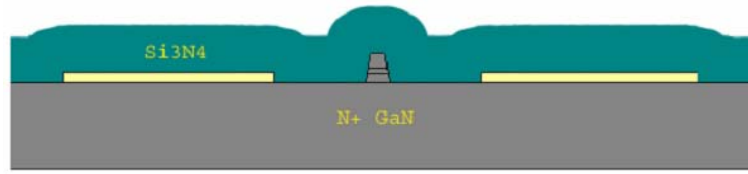


(b)

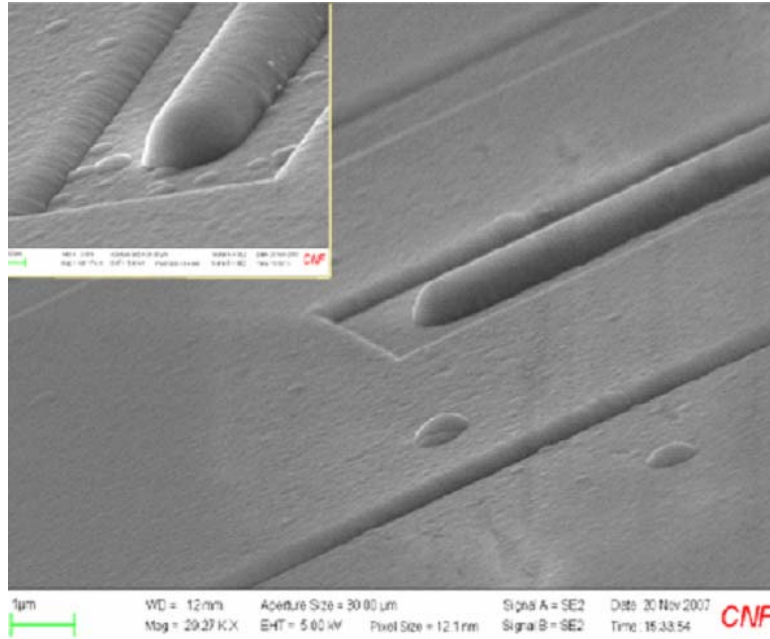
Figure 3.9: (a) Cross-sectional view of the cathode contact (b) SEM photograph

### 3.3.1.3 $\text{Si}_3\text{N}_4$ Planarization

The planarization process begins with conformal deposition of low-stress  $\text{Si}_3\text{N}_4$  thicker than the mesa height. The deposition is performed in the GSI PECVD tool at  $400^\circ\text{C}$  temperature and is rich in silicon. The chamber is conditioned before the actual deposition by running the process on a dummy silicon wafer. This is extremely important for a homogeneous layer from top to bottom since etching characteristics can vary if this is not ensured.



(a)

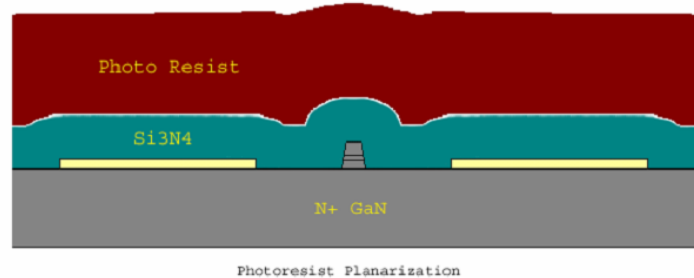


(b)

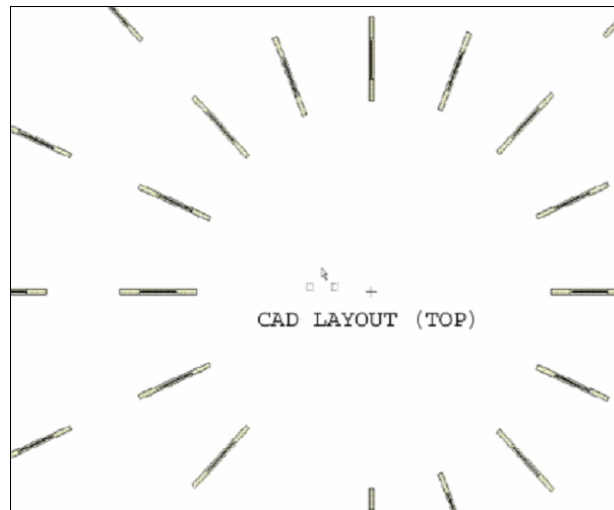
Figure 3.10: Conformal  $\text{Si}_3\text{N}_4$  deposition. (a) Cross-sectional view. (b) SEM image - Insert shows a close-up image.

Next, Shipley 1800 series g-line photoresist is spun atop the  $\text{Si}_3\text{N}_4$  to a thickness that is greater than twice the GaN mesa thickness. As illustrated in Figure 3.11, this thickness safely prevents the side walls of the mesa from being exposed below the ballistic region and get shorted. Photoresist soft baking is avoided at this stage to prevent further hardening of the mask which could potentially preclude the achievement of 1:1 selectivity necessary for the next step. To prevent resist streaking during spin-coating (to achieve maximum planarity and thus device uniformity), the mesas are distributed in the radial direction (in alignment with its longer dimension) in

a circular pattern on the chip. This is shown in Figure 3.11b. Effort has to be made to center the chip on the spinning chuck before dispensing the photoresist. This is accomplished by spinning the chip at low rpm while adjusting its position by nudging with a tweezer. The visible metal traces are large enough to serve as a visual queue to determine by eye if the chip is off center. A P10 measurement right after the spin coat shows ~80 nm smoothened step height compared to ~500 nm height mesa lying underneath.



(a)

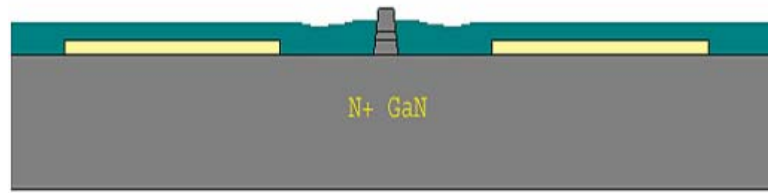


(b)

Figure 3.11: Planarization step (a) Cross-sectional view of planarizing photoresist (b) The radial distribution of devices on the chip to prevent resist streaking.

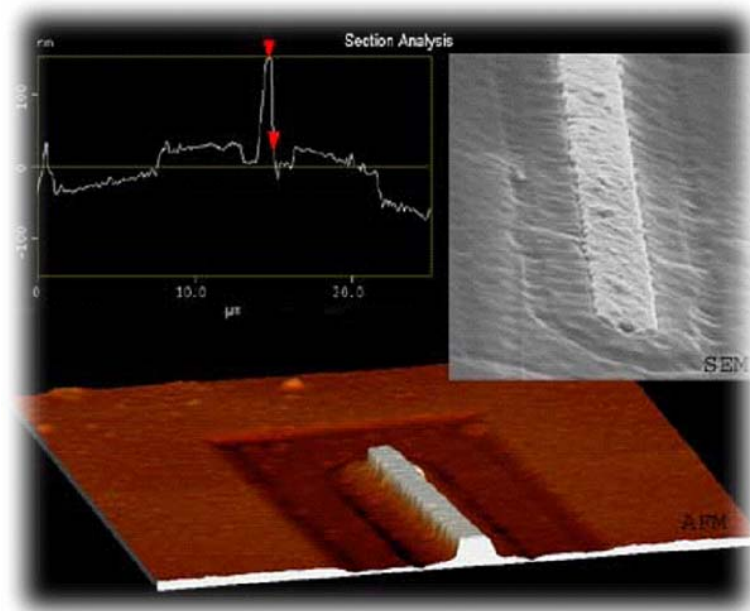
An RIE recipe is optimized to yield approximately 1:1 selectivity between the photoresist (i.e. Shipley 1813) and GSI PECVD low-stress  $\text{Si}_3\text{N}_4$ . DOE experiments with Si witness samples were performed with small photoresist openings atop  $\text{Si}_3\text{N}_4$  to measure and also account for the possible aspect ratio dependence of the selectivity. This possibility had to be tested and eliminated since it could introduce varying contact areas on the diodes and some of them could even be shorted. Film thickness on the actual GaN samples was monitored using F20 Filmetrics optical interferometer tool atop the cathode level contacts (which has 15 nm titanium on top), because measurements proved to be possible and accurate enough through the available titanium calibration data in the software. This is an issue because GaN is difficult to characterize for accurate optical interferometer measurements as opposed to silicon. The bulk of the photoresist is first etched using  $\text{O}_2$  plasma. The final stage of the etch is done using the previously developed 1:1 selectivity recipe. This critical step is conducted in stages. At each stage, the thickness of the resist is monitored by interferometer. Final confirmation of the created structure is obtained by AFM as shown in Figure 3.12.





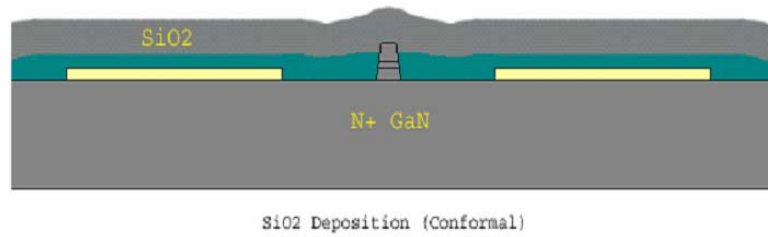
Planarization Step 2 - Etch Back

(a)

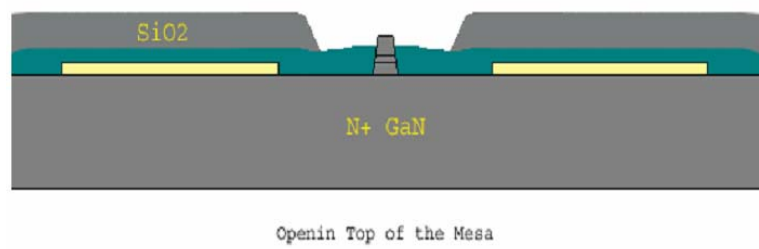


(b)

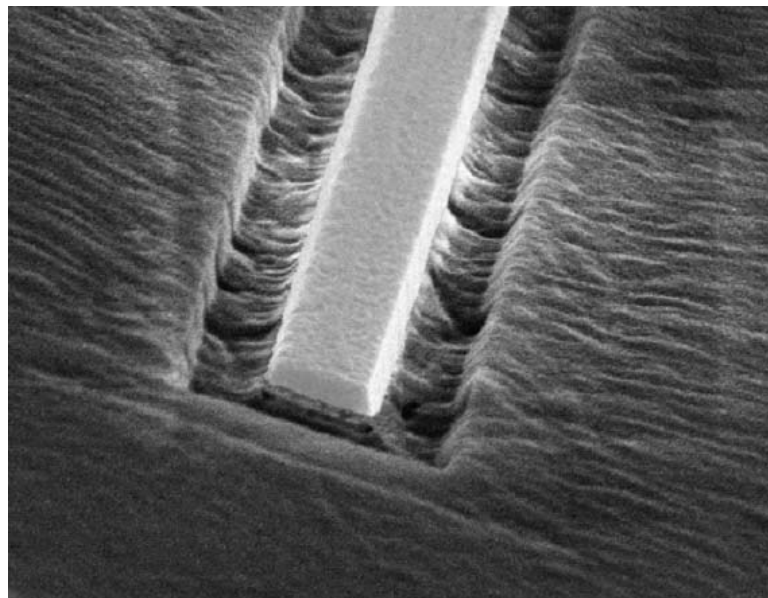
Figure 3.12: Planarized  $\text{Si}_3\text{N}_4$  (a) Cross-sectional view of the planarized diode (b) AFM scan result – 3D topology. Vertical measurements confirm the target depth reached.



(a)



(b)



(c)

Figure 3.13: Oxide isolation step (a) Cross-sectional view after conformal SiO<sub>2</sub> deposition. (b) Cross-sectional view after opening the mesa for electrical contact. (c) SEM image of the final structure before metallization

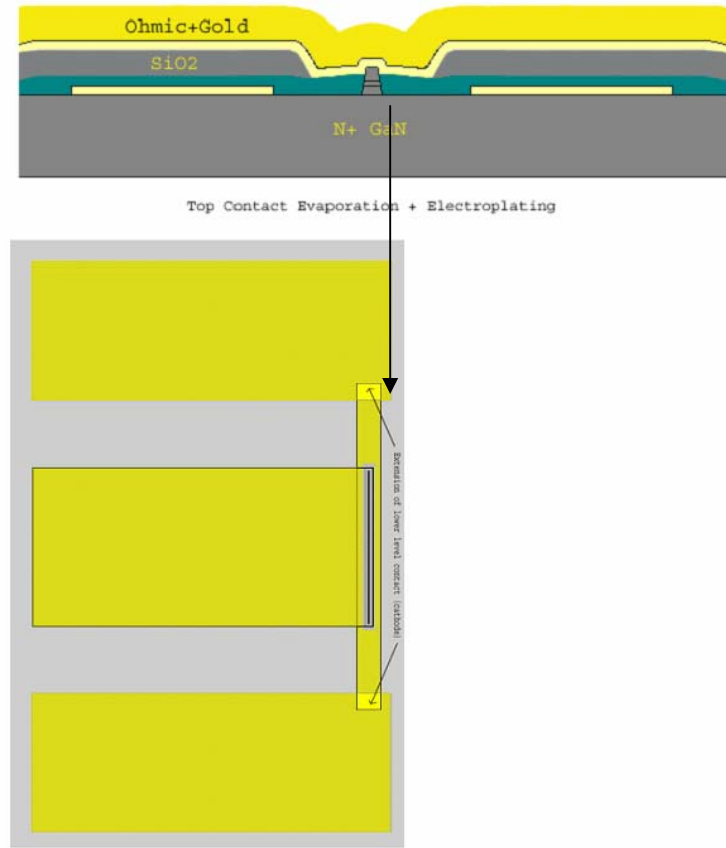
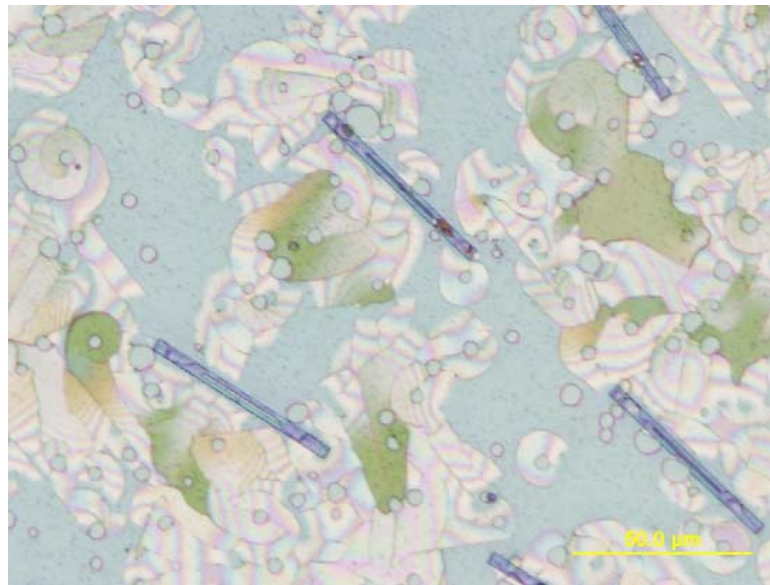


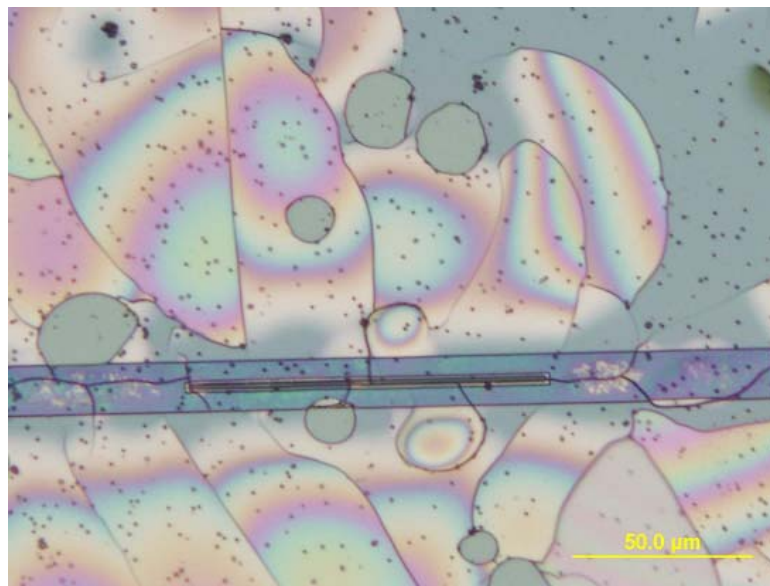
Figure 3.14: Final structure (a) Cross-sectional view of the final structure. (b) Top-view showing the contact pads.

$\text{Si}_3\text{N}_4$  planarization is followed by  $\text{SiO}_2$  deposition. Without  $\text{SiO}_2$ , remaining planarized high-k  $\text{Si}_3\text{N}_4$  is too thin ( $\sim 70$  nm on the cathode contact) separating the two overlapping electrodes and this raises a concern about very high parasitic capacitance. Permittivity of  $\text{SiO}_2$  is  $\sim 3.7$  and, a 200 nm high layer was included in the design to minimize this parasitic capacitance.

$\text{SiO}_2$  on top of the mesa is etched away for electrical access. It is achieved by first a dry etch then wet etch using diluted HF (30:1) to have high selectivity between  $\text{Si}_3\text{N}_4$  and  $\text{SiO}_2$ .



(a)



(b)

Figure 3.15: Optical microscope photographs (at different magnifications) showing the  $\text{Si}_3\text{N}_4$  layer destroyed by the rapid thermal annealing.

A separate etch step is necessary for both opening the extension of the cathode for ground pad metallization (for cascade probing) and top contact TLM test patterns since  $\text{Si}_3\text{N}_4$  thickness outside the device area is thicker as a result of photoresist planarization.

#### **3.3.1.4 Ohmic Contacts**

Anode ohmic contacts are delineated using e-beam lift-off technique. A final layer of 400 nm thick gold is used to facilitate heat spreading through the metal contacts. When the anode ohmic contact is put in place, they need to be annealed at  $\sim 800^\circ\text{C}$  (which simultaneously anneals the cathode contacts). Note that the  $\text{Si}_3\text{N}_4$  layer is deposited at  $400^\circ\text{C}$  and initial experience later showed that rapid thermal annealing at  $\sim 800^\circ\text{C}$  shatters and destroys this layer due to hydrogen out-diffusing which was trapped during the deposition. This damage in question is shown in Figure 3.15.

Experiments were done to remedy this situation and it was found that programming the RTA to increase temperature by  $50^\circ\text{C}$  every 40 seconds starting from  $400^\circ\text{C}$  until  $800^\circ\text{C}$  leaves the  $\text{Si}_3\text{N}_4$  intact and still accomplishes the ohmic anneal.

## CHAPTER 4

### Quasi-ballistic NDC diodes

#### 4.1 Introduction

A seminal femto-second optical pulse-probe experiment by Wraback et al. [8, 28] determined the high electron velocity reached in high electric fields over short distances. The electron accumulation layers (EAL) generated by ultra-short optical pulses was nearly ballistically accelerated to a peak velocity of  $\sim 7 \times 10^7$  cm/sec (maximum possible group velocity limited by the GaN band structure is  $\sim 8 \times 10^7$  cm/s. [8]). The finite optical pulse length of  $\sim 70$  fs, and the spatial energy spread in Wraback's experiments are partially limiting the apparent peak measured velocity reached. Although his experimental p-i-n device had a  $1 \mu\text{m}$  intrinsic layer drift region, most of the interesting results occurred over the first 250 nm of this distance. The EAL position was measured as a function of time as it was moving under the influence of several different values of electric field strengths ranging from 81 kV/cm to 543 kV/cm. This allowed the determination of the EAL drift velocity as a function of time through differentiation. High field velocity-time curves taken from [8] are shown in Fig.1. In this article, an analytical expression for the electron drift velocity,  $v_D(E)$ , as a function of applied electric field is derived from these data and incorporated into the simulations to characterize the high field transport for the selected 125 and 250 nm long channel diodes.

The derivation was carried out by first determining the time-delay for traversing a selected diode channel length (125 or 250 nm) for a given field strength, and

averaging the drift velocity within that interval. Repeating this procedure for all 7 field strength data published in [28] and [8], the discrete points in Figure 4.2 are obtained and an analytical function is fit to these data points.

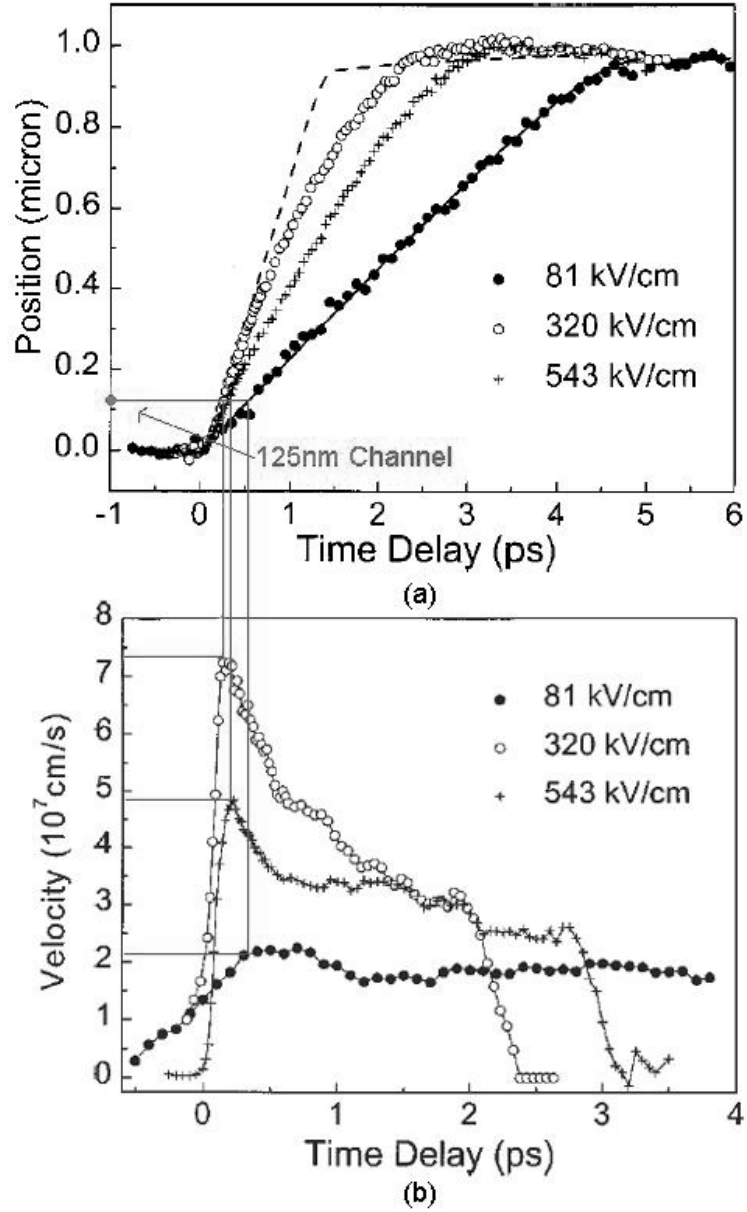


Figure 4.1: Measured (a) EAL position vs. time. (b) EAL drift velocity vs. time. The data shown in (a) and (b) are taken from [1]. Four other field strength measurements are also available in [2].

The average velocity for a 125 nm diode has a peak value of  $7 \times 10^7$  cm/s near 295 kV/cm electric field and falls to  $4 \times 10^7$  cm/s at 543 kV/cm. This reduction may extend well beyond this field strength.

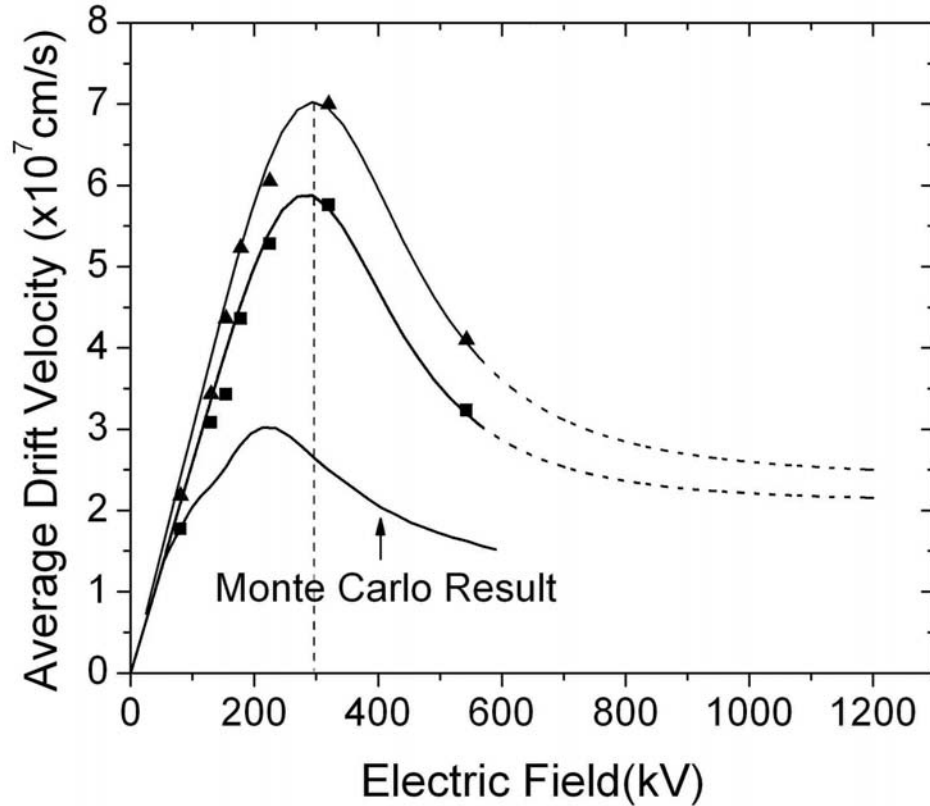


Figure 4.2: Velocity-field characteristics of the selected 125 and 250 nm long channels derived from [1,2]. Solid curves show the analytical fit to the discrete points representing experimental data. The dashed portions indicate the extrapolated values. Monte Carlo results published in [2] are also shown in contrast to these transient effects. These Monte Carlo results are valid for steady-state transport in bulk material and ignore the finite LO phonon lifetime which causes significant reduction in the peak velocity.

Although separate measurement times for electrons to transfer to upper valleys and back have been determined for GaN [20], as well as the longitudinal optical (LO) phonon launch time in the central ( $\Gamma$ ) valley, these effects do not need to be analyzed separately here, since the measurements reported by Wraback et al. include all such



physical effects. His experiments give a velocity reduction time of 0.25-0.3 ps, which is not far from the measurements reported in [20]. That time rate of velocity reduction likely involves electron transfer to the upper valleys, negative electron mass effect, electron reflection at the Brillouin zone boundary, and build up of LO phonons [10, 11]. Due to the ultra-short drift time, most electrons that reach the upper valleys are predicted to lack enough time to return to the central  $\Gamma$  valley.

This ultra-short channel length and high electric field operation has properties similar to those in the Gunn diodes for average electron velocity vs. electric field, but involves much more complex transient physical and quantum electronic properties [29-31]. Also shown in Fig.2 is a typical Monte Carlo result on GaN velocity-field characteristics [8]. The difference in the peak velocities due to transient ballistic effects is clearly seen in this figure. The work presented in this paper is an improvement upon previous studies on submicron length diodes in which the transport was solely based on the Monte Carlo results [32]. Furthermore, Monte Carlo simulations in general do not take into account the finite  $\sim 350$  fs life-time of the LO phonons [5]. Experience in HEMT channels [33, 34] and theory by Ridley et al. [10] shows that peak drift velocity is  $\sim 1.0 \times 10^7$  cm/s or less in GaN.

In a properly loaded resonant circuit, EALs can periodically be drawn from the heavily-doped cathode  $n^+$  layer and ballistically accelerated into the drift region. Under different bias conditions and doping-frequency ratios, the diode can be operated at and above the transit-time frequency. In the latter case, the circuit quenches the EAL before reaching the anode.

In order to meet the doping-length ( $N_D L$ ) product criterion (discussed later) and generate significant ac power, the doping in the designs discussed in this article (Figure 4.3) is chosen to be  $1 \times 10^{18} \text{ cm}^{-3}$ . The applicability of the  $v_D(E)$  relation at  $1 \times 10^{18} \text{ cm}^{-3}$  doping level, (which was constructed from measurements performed in a  $1 \times 10^{15} \text{ cm}^{-3}$  doped sample) is justified by the fact that the drift velocity of hot electrons is only minimally affected by the impurity scattering at high electric fields which has been verified in GaN by Monte Carlo simulations [35]. Moreover, from a fabrication perspective,  $1 \times 10^{18} \text{ cm}^{-3}$  is appropriate since typical (MBE) doping profiles are significantly more reproducible above  $\sim 5 \times 10^{17} \text{ cm}^{-3}$ .

## 4.2 Simulation Method

The geometry of the GaN diode studied in the simulations is shown in Figure 4.3. For computational efficiency and separation of the large geometric capacitive current  $I_{CD}$  from that of the electronic current  $I_D$ , the diode was modeled as a one dimensional (1D)  $n^{++}$ - $n$ - $n^{++}$  structure in parallel with its geometric capacitance. The capacitance values for the selected 125 and 250 nm diodes are calculated from a two-dimensional (2D) small-signal finite element analysis of the corresponding geometries and found to be 4.22 and 3.45 fF respectively. These capacitance values are dominated by the fringing fields penetrating the undoped GaN as a result of its high dielectric constant compared to air.

The  $n^+$  regions in the design facilitate good ohmic contacts with the physical diode and, at the cathode-side, provide the necessary electron concentration gradient for the periodic nucleation of the EALs.

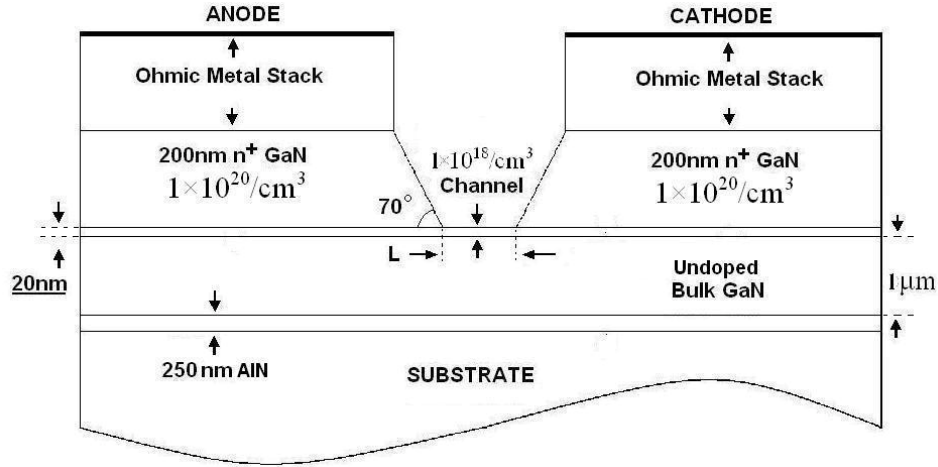


Figure 4.3: Cross section of the diode geometry.

This model is then placed in a circuit in parallel with an inductor and a load resistor as shown in Figure 4.4. Simultaneous solution of Kirchoff's equations in nodal form follows (with zero initial conditions) and, for each instantaneous value of the anode voltage of the diode (which constitutes a boundary condition for the internal transport equations), simultaneous solutions of the Poisson and current continuity equations, (4.1) and (4.2), are obtained within the diode using the physics-based "Atlas" device simulator (Silvaco Inc.)

$$\frac{\partial E}{\partial x} = q \frac{(n - N_D)}{\epsilon_r \epsilon_0} \quad (4.1)$$

$$\frac{\partial J}{\partial x} = -\epsilon_r \epsilon_0 \frac{\partial E}{\partial t} \quad (4.2)$$

The transport is described by the drift-diffusion approximation with its velocity field characteristic,  $v_D(E)$ , as depicted in Figure 4.2.

$$J = qn v_D(E) - qD_n \frac{\partial n}{\partial x} \quad (4.3)$$

The spatial and temporal mesh sizes were chosen according to (4.4) and (4.5) in order to ensure the accuracy of the solutions. [36].

$$\Delta t \leq \tau_{\varepsilon} \quad (4.4)$$

$$\Delta x \leq v\tau_{\varepsilon} \quad (4.5)$$

Here  $\tau_{\varepsilon}$  is the dielectric relaxation time and  $v$  is the electron velocity in the cell. Inequality (4) implies that the time steps should be much shorter than the dielectric relaxation time characterizing the exponential growth rate of the EAL. Similarly (5) ensures the spatial resolution of the EAL within a dielectric relaxation time.

Note that this is a quasi-static approximation which assumes that the drift velocity instantaneously follows the local electric field. In reality, velocity-field characteristics are always a function of the displacement current due to the finite kinetic relaxation times associated with the intervalley transitions. In collision dominated transport, this dependence is particularly important at frequencies approaching

$$f = \frac{1}{\tau_{ER} + \tau_{ET}} \quad (4.6)$$

Here,  $\tau_{ER}$  is the energy relaxation time and  $\tau_{ET}$  is the intervalley relaxation time [37]. However, in the proposed ultra-short BEAN diodes, not only are there apparent ballistic electrons involved in the transport [14, 15, 20, 38], but also, the electrons transferred to the satellite valley are not likely to have enough time to scatter back to the  $\Gamma$  valley [3] before being collected at the anode, eliminating the longer component of the intervalley transition delay. Thus, the quasi-static approximation is justified, giving these devices a tremendous potential for efficient THz generation.

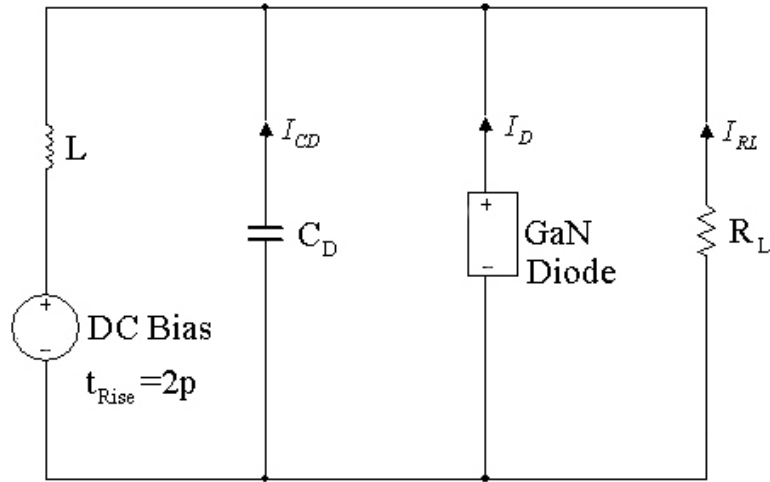


Figure 4.4: Parallel resonant circuit topology used in simulations. dc bias rise-time is 2ps.  $C_D$  represents the geometric capacitance and  $R_L$  is the load resistance.

### 4.3 Theoretical Background on EAL Dynamics

Given the quasi-static velocity-field assumption, the general analysis techniques of transferred electron based NDC diodes can be used to study the electron dynamics in these diodes. The pertaining literature is extensive [36, 39-41]; here, only the basic concepts which are central to device operation are outlined.

As predicted directly by (4.1), (4.2) and (4.3), when the average bias field in the channel rises above the threshold value and the inequalities (4.9), (4.10) and (4.11) are more or less satisfied, exponentially growing EALs nucleate at the cathode and propagate toward the anode (In Figure 4.5a, such results are shown and will be discussed in the next section)

As a result of these EALs (or dipole domains), it is extremely difficult to measure a static current-voltage curve that follows the velocity-field relation unless one uses short enough pulsed biasing – in the order of dielectric relaxation time - to prevent EAL growth. Sub-critical doping (primarily used for amplifiers) on the other hand

prevents these instabilities; however, static NDC is still inaccessible due to the development of *static* non-uniform space charge distribution in the sample when biased above its threshold [15, pp 48].

An insightful analytical expression  $n(x, t, k)$  as an approximate solution to (4.1), (4.2) and (4.3) in the small signal condition can be found in [36].

$$n(x, t, k) \propto \exp(-t/\tau_\varepsilon) \exp(-D_0 k^2 t) \exp jk(x - v_a t) \quad (4.7)$$

where  $\tau_\varepsilon$  is the dielectric relaxation time, and;

$$\tau_\varepsilon \equiv \frac{\varepsilon_r \varepsilon_0}{q N_D (\partial v_d / \partial E)} \quad (4.8)$$

Here,  $n$  is the electron concentration,  $N_D$  is the doping in the channel,  $D_0$  is the diffusion coefficient,  $v_a$  is the drift velocity of the EAL, and  $k$  is the wave number. It is clear from (4.7) and (4.8) that negative values of  $\partial v_d / \partial E$  imply the growth, rather than dissipation, of disturbances in the neutral space-charge distribution.

The periodic nucleation and collection of these EALs at the anode creates current-voltage oscillations at the terminals of the diode at a frequency which is, to first order, determined by the average transit time of the EAL across the channel. Furthermore, at steady state, there is always an ac voltage superimposed on the dc bias voltage and thus the amplitude and phase of these oscillations depend strongly upon the external circuit. In order to create the electrodynamic behavior described above, certain design criteria, given by (9), (10) and (11), must be considered [39].

$$N_D L > \frac{2 v_0 \varepsilon \varepsilon_0}{e |\partial v / \partial E|} = 2.1 \times 10^{12} \text{ cm}^{-2} \quad (4.9)$$

$$N_D L^2 > \frac{\epsilon \epsilon_0 D \pi^2}{e(\partial v / \partial E)} = 0.3 \times 10^7 \text{ cm}^{-1} \quad (4.10)$$

$$N_D d > 2 \times 10^{11} \text{ cm}^{-2} \quad (4.11)$$

In these equations,  $L$  is the channel length,  $d$  is the thickness of the channel,  $N_D$  is the channel doping,  $D$  is the diffusion coefficient,  $e$  is the electronic charge and  $\partial v / \partial E$  and  $v_0$  are the average negative differential mobility and the average EAL velocity at the operating bias point, respectively. Calculated values for GaN for the 125 nm diode as follows:  $N_D L = 12.5 \times 10^{12} \text{ cm}^{-2}$ ,  $N_D L^2 = 1.56 \times 10^8 \text{ cm}^{-1}$  and  $N_D d = 2.0 \times 10^{12} \text{ cm}^{-2}$ .

Satisfaction of condition (4.9) is necessary for the EALs to grow to maturity. Condition (4.10) is related to the diffusion effects. Indicated by (4.7), the diffusion causes distortion in the shape of the EAL. When (4.10) is satisfied, the accumulating force of the negative dielectric relaxation time will dominate over the dispersing force of the diffusion so that EALs may grow.

It should also be noted that the electric field outside the channel, produced by an EAL inside, acts to restore the charge distribution to a uniform state, opposing the formation of the EAL. For a sufficiently thin channel, the effect is important [39], and the criterion is given in equation (4.11)

#### 4.4 Results And Discussions on a 125 nm Diode

Numerous bias voltage and load resistance combinations for 125 and 250 nm devices have been studied and collective results will be presented in the next section. In Figure 4.5, only the important internal parameters for a particular 125 nm diode design are

shown and discussed. The diode and circuit parameters used for this simulation are tabulated in Table I.

Table 4-1: Simulation Parameters

Parameter	Value
Channel length	125 nm
Channel thickness	20 nm
Channel doping	$1 \times 10^{18} \text{ cm}^{-3}$
Device Width	50 $\mu\text{m}$
Load Resistor	220 $\Omega$
Bias	10 V
Fundamental Frequency	2.9 THz
ac output power	0.5 W/m
dc power dissipation	22.5 W/mm
Phase angle difference	$72^\circ$
Efficiency	2.2 %
Quality factor ( 4.2fF//0.6pH)	18.3
$V_D$ peak to peak	6.7 V
$I_D$ peak to peak	2 A/mm
$I_{CD}$ (geometric capacitance)	10.5 A/mm

Figure 4.5a illustrates the nucleation and propagation of the EALs (for one oscillation cycle) as a function of time. The EAL is on average two room-temperature Debye lengths wide with its peak density saturating at  $\sim 2 \times 10^{19} \text{ cm}^{-3}$ . The insert shows the average velocity of the EAL over time; the peak velocity in this case is rather small compared to the values shown in Figure 4.2 due to the high bias voltage. Furthermore, the maximum field strength in the vicinity of the anode region is  $\sim 3.0 \text{ MV/cm}$ ; however, the concern of the avalanche breakdown is mitigated due to the narrow spatial extent of these fields as shown in Figure 4.5(b). In order for breakdown to



occur, the total energy absorbed by the ballistic electrons,  $E \times \lambda_m$  ( $\lambda_m$  is the approximate mean free path and  $E$  is the electric field) should exceed the band gap energy of 3.4 eV roughly by 50 %, which is  $\sim 5.1$  eV.

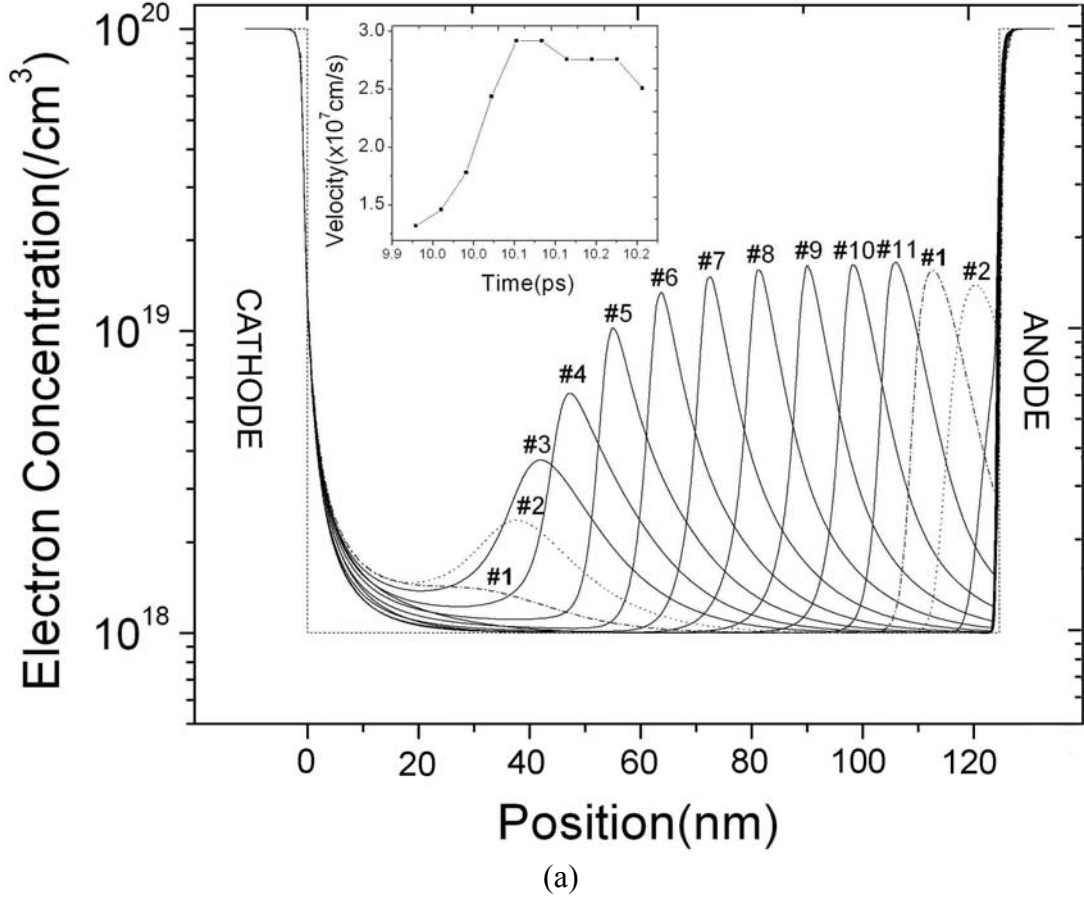
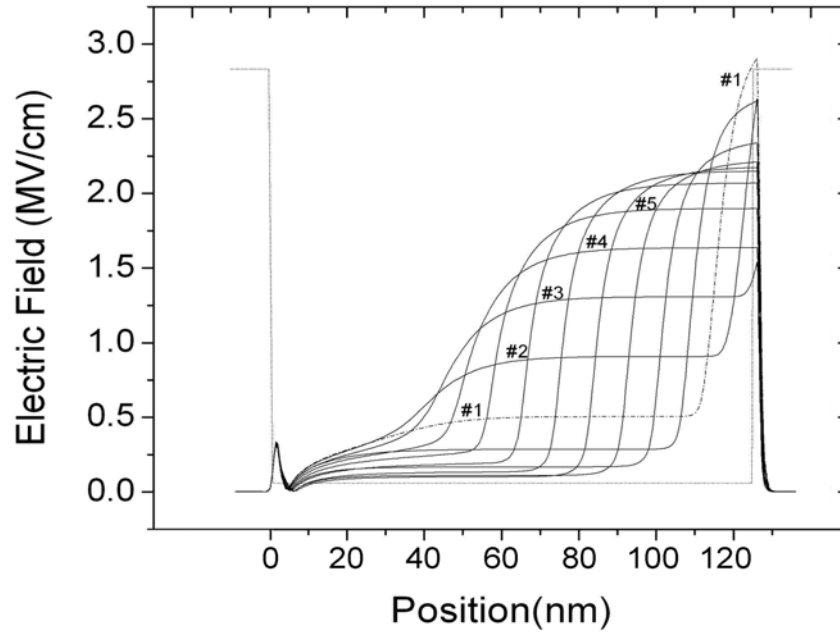
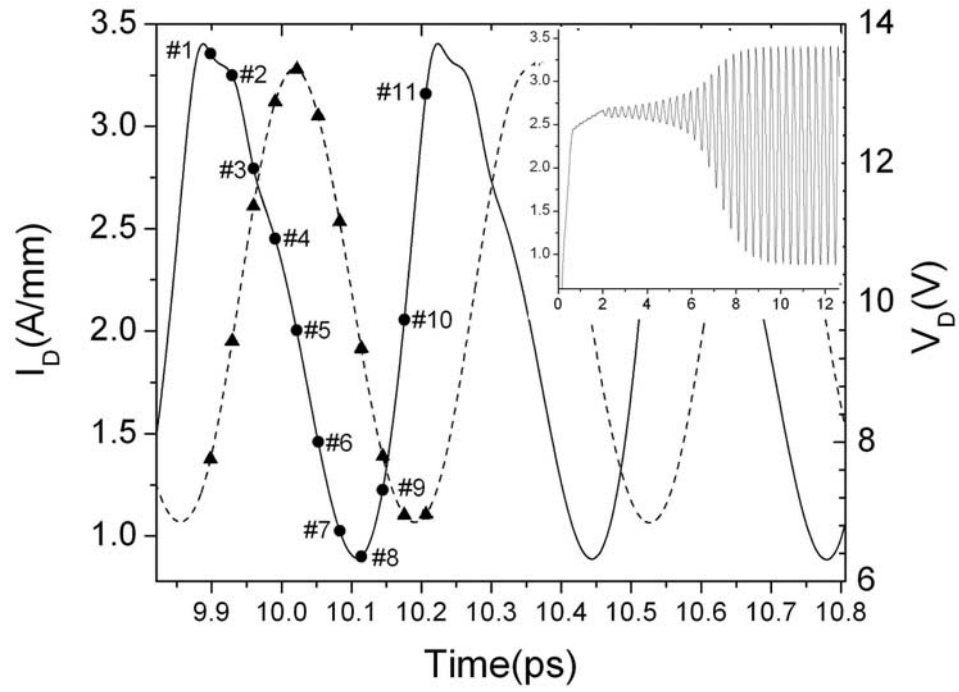


Figure 4.5: (a) Electron concentration vs. position at successive instances of time showing EALs in transit moving towards the anode. Background doping is shown dashed. Insert shows the average EAL velocity as a function of time. (b) Electric field vs. position. For both (a) and (b), each numbered curve represents an instant of time and they are 30 fs apart. (c) Anode current-voltage waveforms as a function of time. Insert shows the build up of the current oscillations. (d) Phase plane plot on the dynamic load line. Insert shows a 250 nm diode. Towards the anode, numbers 1 and 2 are repeated since they are, at that particular instant, the accumulation layers which are about to leave while a new one is nucleating.

Figure 4.5 continued

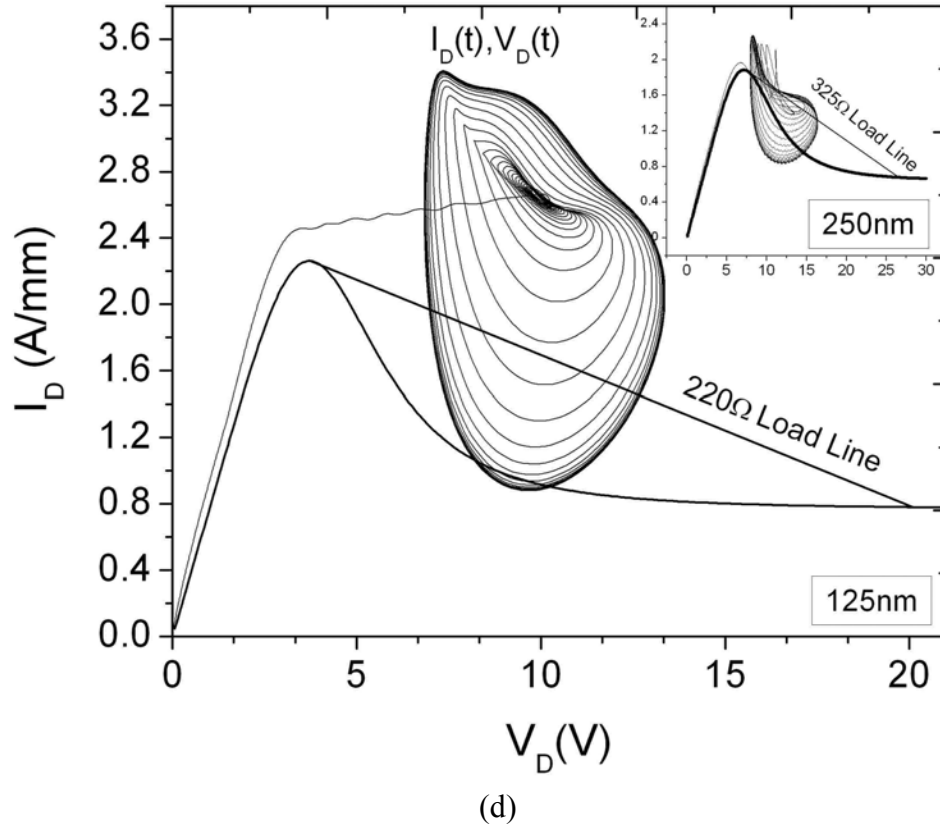


(b)



(c)

Figure 4.5 continued.



In Figure 4.5(c) insert, it is also seen that the number of cycles required to build up the oscillations is approximately equal to the circuit quality factor of  $\sim 18$ . Shown in Figure 4.5(d) is the phase plane plot of the  $I_D$  and  $V_D$  as a function of time. The current contribution due to injected space charge is more pronounced for the shorter diode.

Table 4-2: Harmonic contents of the oscillator output

Harmonic (THz)	I (A/mm)	V(V)	P (W/mm)	Theta
2.88 (1 <sup>st</sup> )	0.98	3.34	0.5	72.1
5.76 (2 <sup>nd</sup> )	0.26	0.1	$3 \times 10^{-3}$	76.6

Harmonic content of the ac power output has been analyzed using the Fast Fourier Transform (FFT) technique with a Kaiser Window function of  $\beta=9$  (Table II) [42].

The sampling and fundamental frequencies were chosen to be 50 THz and 2 GHz, respectively, in order to satisfy the Nyquist criterion. As indicated in Table II, the current has a rather significant second harmonic, while voltage is nearly sinusoidal, consistent with the well known characteristics of high-Q oscillators.

#### 4.5 Collective Results And Discussions

NDC oscillators based on space-charge instabilities present an extremely nonlinear mathematical problem. With today's computational resources however; a brute-force approach of simulating selected combinations of parameters to identify trends and understand the diode operation as part of the circuit environment is possible. In this section, results of such selected combinations of bias-load parameters are presented for both diode lengths. For each combination, the efficiency was maximized through many iterations tuning the parallel inductor. The bias-load combinations were chosen based on a load line analysis using an I-V curve constructed by scaling the corresponding velocity field relation. A comparison of the NDC diode characteristics for the two diode lengths is shown in Table III.

Table 4-3: NDC Diode Characteristics

Parameter <sup>a</sup>	125 nm	250 nm
Threshold Bias Voltage	3.7 V	7.2 V
Peak to Valley Ratio	2.8	2.7
Low Field Conductance	0.037 S	0.017 S
Max. Negative Conductance	0.020 S	0.009 S

<sup>a</sup>50  $\mu\text{m}$  device width is assumed.

Following in this section are discussions of key conclusions drawn from collective these simulation results.

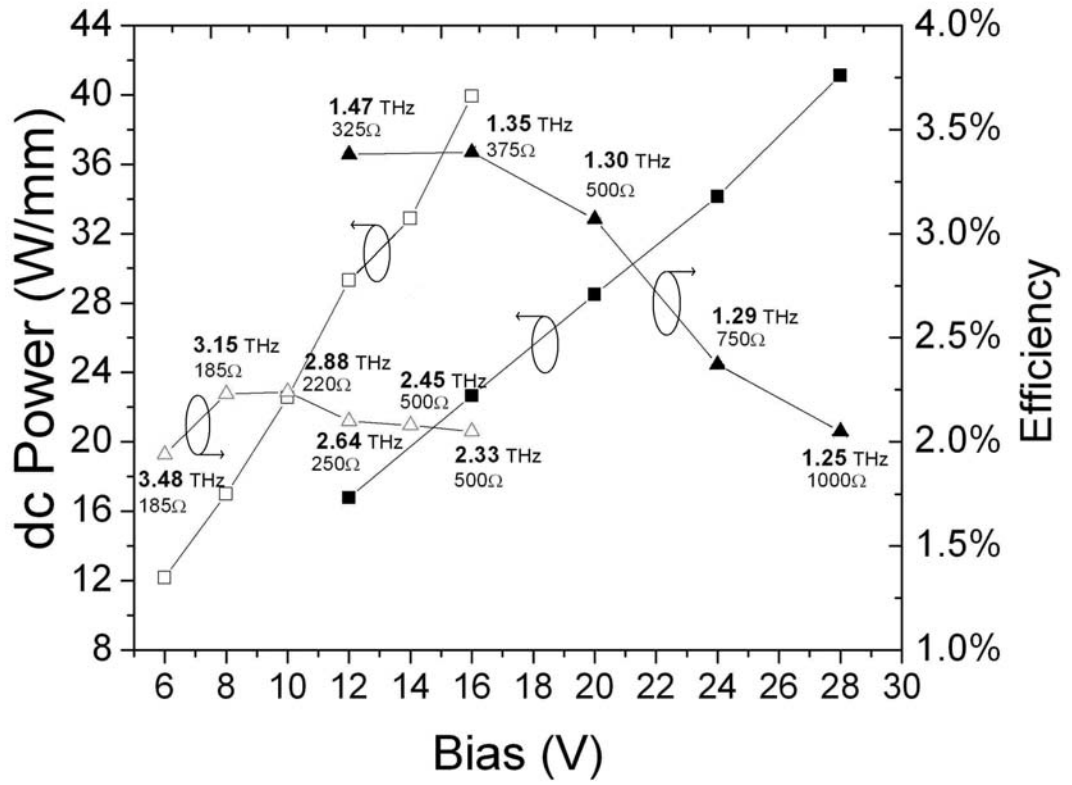


Figure 4.6: Efficiency and dc power dissipation comparison between 125 (open) and 250 nm (closed) diodes as a function of bias voltage. All the diodes are 50  $\mu\text{m}$  wide. Each load-bias combination is tuned with the parallel inductance for maximum efficiency. Corresponding oscillation frequencies (fundamental) and load resistance values are also labeled on each data point.

#### Efficiency monotonically decreases with increasing bias voltage

When bias is increased, the efficiency decreases despite the increasing ac power output. This is caused by the faster increase in the dc power dissipation. The conversion efficiency here is defined as the ratio of ac power delivered to the load and the dc power dissipated in the GaN diode. Consistent with the load line perspective, the trend is that, as the bias voltage is increased, the optimum load resistance yielding the maximum efficiency also increases; this, in turn, increases the peak-to-peak amplitude of the voltage and current swings despite the fact that the phase difference

monotonically approaches 90 degrees from below, at which no power can be generated. The amount of dc power dissipation is considered critical for the important role it plays in determining the channel temperature from a practical point of view and, transient thermal presentations will be presented and discussed in section VII.

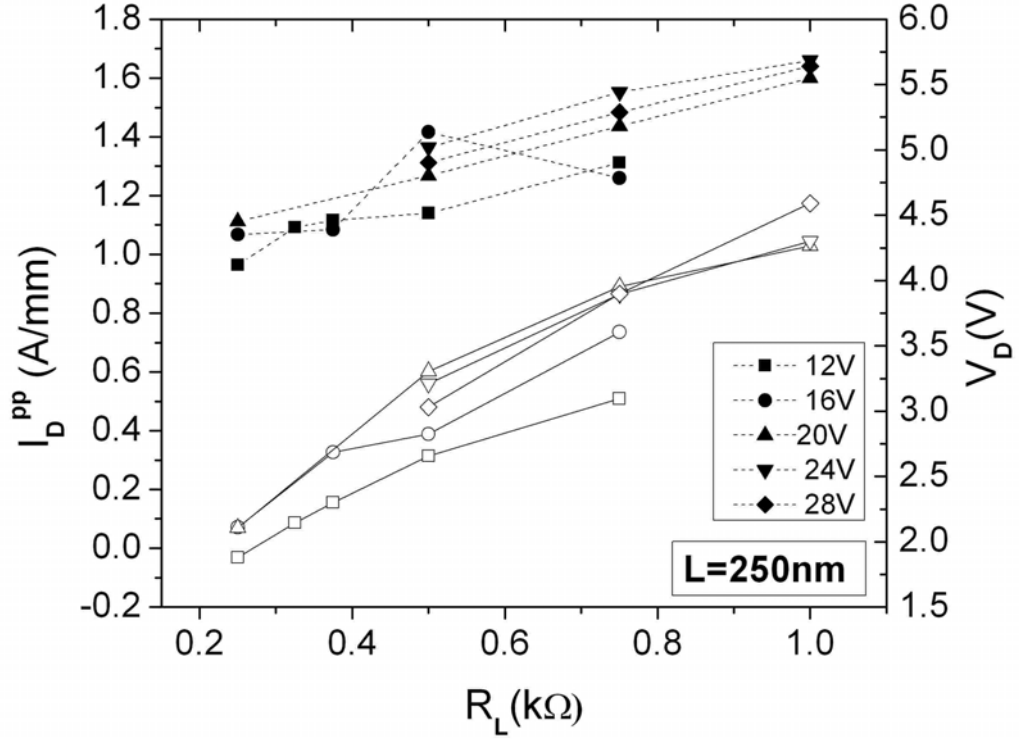


Figure 4.7: Peak to peak current (closed) and voltage (open) oscillation amplitudes as a function of load resistance.

#### Oscillation frequency decreases with increasing bias voltage

As shown in Figure 4.8, decrease in frequency is a result of the higher (average) electric field across the diode, effectively slowing the EALs in transit. This trait of bias tunability is very desirable. Moreover, cold circuit resonance frequencies calculated from

$$f_R = \frac{1}{2\pi\sqrt{LC}} \quad (4.12)$$

are also shown in Figure 4.8. The contribution from the non-linear capacitance of the channel is apparent from the EAL dynamics; however, the difference between cold resonance calculations and actual oscillation frequencies remain approximately constant.

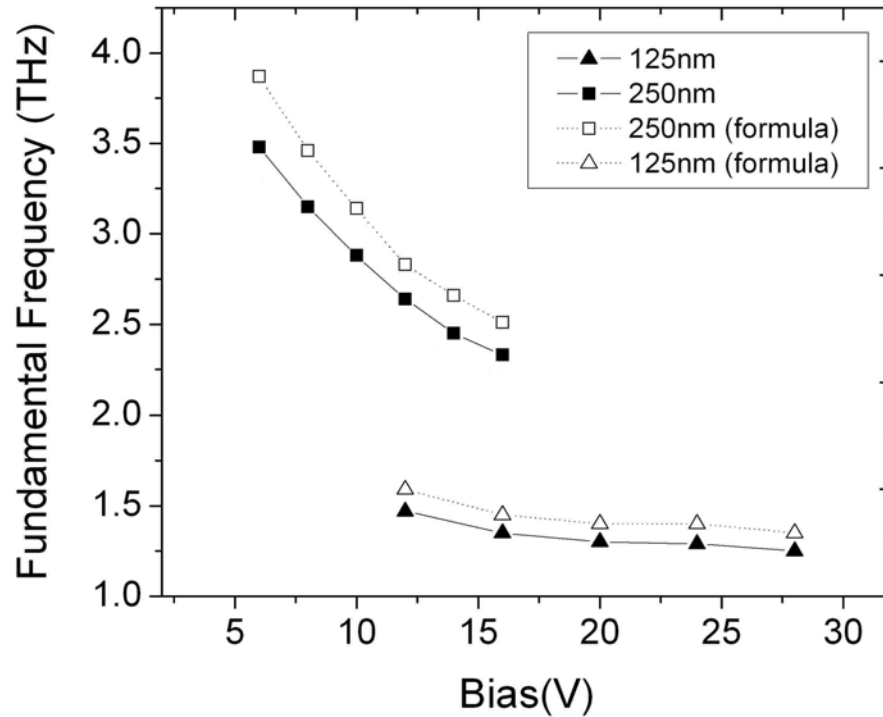


Figure 4.8: Fundamental oscillation frequency vs. bias voltage and cold resonance frequency calculations for 125 (open square) and 250nm (open triangle). Comparison illustrates the influence of the nonlinear capacitance of the channel.

#### **dc Power dissipation levels are similar for both 125 and 250 nm diode lengths**

The 250 nm diode requires about twice the bias voltage compared 125 nm; however, the dc Power dissipation levels are quite similar. The increased space-charge limited current is responsible for this through compensating for the lower threshold voltage in the  $P=IV$  power expression.

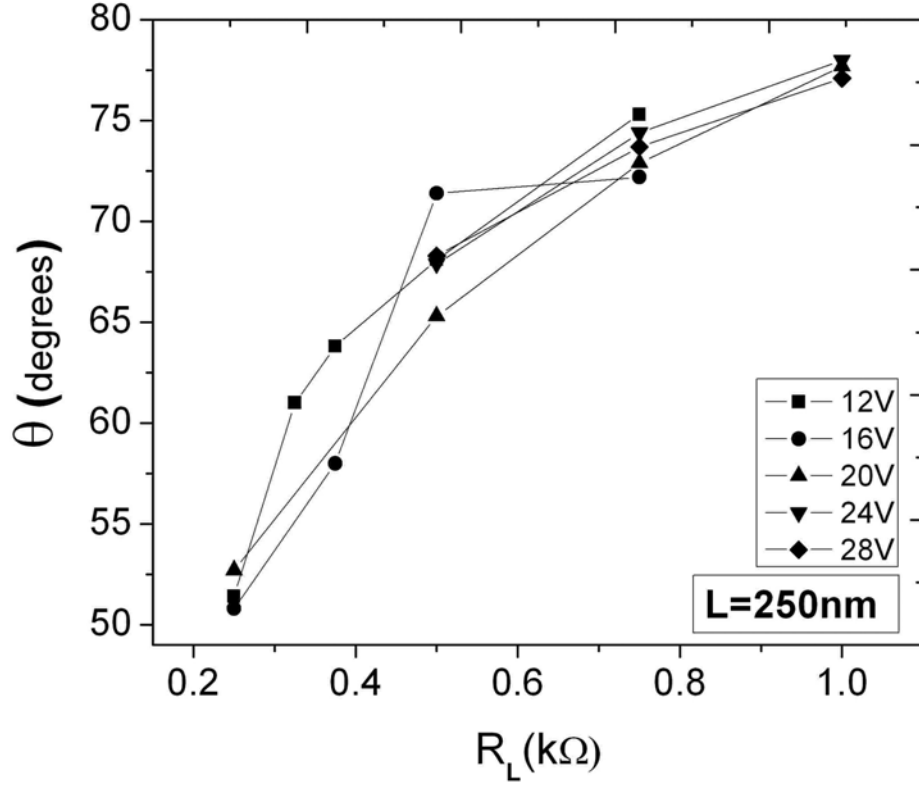


Figure 4.9: Phase angle difference between the diode current  $I_D$  and voltage  $V_D$  as a function of the load resistance (250 nm diode)

#### 4.6 Stationary Accumulation Layer Condition

When the tank circuit frequency is set significantly different from that of the transit time, it has been observed that the periodic formation and collection of the EALs cannot be sustained in the diode. This leads to a stationary EAL condition after a few initial oscillation cycles [43, 44] as shown in Figure 4.10 insert.



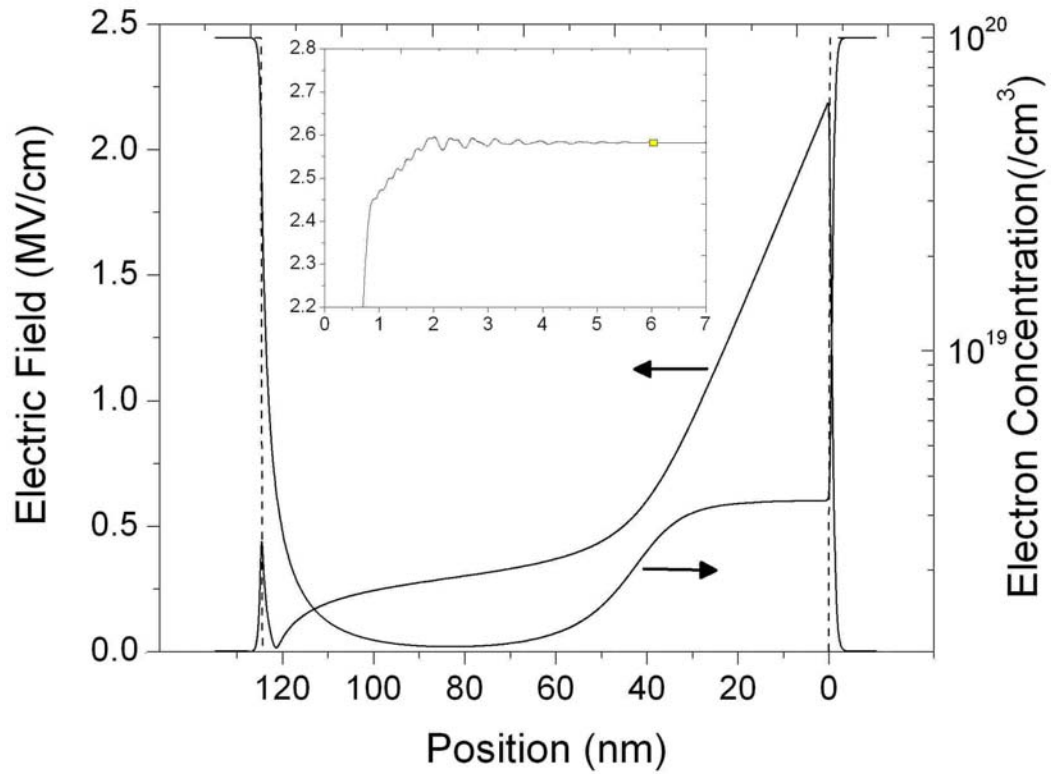


Figure 4.10: Stationary EAL and the corresponding electric field distribution within a 125 nm diode. The bias voltage is 8 V, load resistance is 125  $\Omega$  and parallel inductance is 0.9 pH. Insert shows the associated terminal current wave form (A/mm) as a function of time.

#### 4.7 Thermal Simulations

One of the challenges we encountered in our research in electronic THz power generation using GaN-based NDC diodes has proven to be the reconciliation of the high current density and high electric field operation requirement with an efficient heat dissipation strategy to prevent excessive heating or, more severely, permanent destruction of the diodes. Substrate thickness (typically several hundreds of microns) and its thermal conductivity play a very important role in determining the channel temperature. Due to the lack of native substrates, materials such as sapphire and SiC are popular as host substrates for GaN epilayers. Despite its inexpensive price, sapphire is not considered appropriate for the fabrication of BEAN diodes with its

room temperature thermal conductivity being  $0.35 \text{ Wcm}^{-1}\text{K}^{-1}$ , an order of magnitude less than that of SiC. Even SiC of usual  $\sim 300\text{-}400 \text{ }\mu\text{m}$  thickness appears to be nonfeasible based on the following thermal simulation results. GaN on chemical vapor deposited (CVD) polycrystalline diamond substrates on the other hand have received a lot of attention recently and have already been experimentally demonstrated to operate significantly cooler than GaN on SiC with its more than  $10 \text{ Wcm}^{-1}\text{K}^{-1}$  room temperature thermal conductivity [45].

In this section, transient thermal simulation results of the proposed BEAN diodes on  $25 \text{ }\mu\text{m}$  (thick) back-side thinned SiC and  $40 \text{ }\mu\text{m}$  thick CVD diamond substrates is compared in terms of channel temperature rise. The (2D) finite element thermal simulations of the geometry (Figure 4.3) were performed using the “Giga” module of the “Atlas” device simulator and simulation parameters are tabulated in table IV. These parameters are tested against experimental measurements (time-resolved Raman thermography) and verified by simulating the identical structure reported in [46].

Table 4-4: Thermal parameters of materials used in simulations  $C_p$  is the specific heat,  $\rho$  is the mass density and  $\kappa$  is the thermal conductivity.

Parameter	GaN	SiC	Diamond
Thickness	$1\mu\text{m}$	$25\mu\text{m}$	$40\mu\text{m}$
$C_p(J/g^\circ C)$	0.49	0.69	0.50
$\rho(g/cm^3)$	6.09	3.21	3.515
$\kappa(Wcm^{-1}K^{-1})$	$2 \times (T/300)^{-0.6}$	$3.5 \times (T/300)^{-1}$	$10 \times (T/300)^{-1}$

In the following thermal simulations, only heat diffusion from the bottom of the substrate is taken into account and heat removal along the contacts has been ignored. For the bottom of the substrate, an isothermal boundary condition of  $0^\circ\text{C}$  has been applied corresponding to the case of a perfect heat sink.

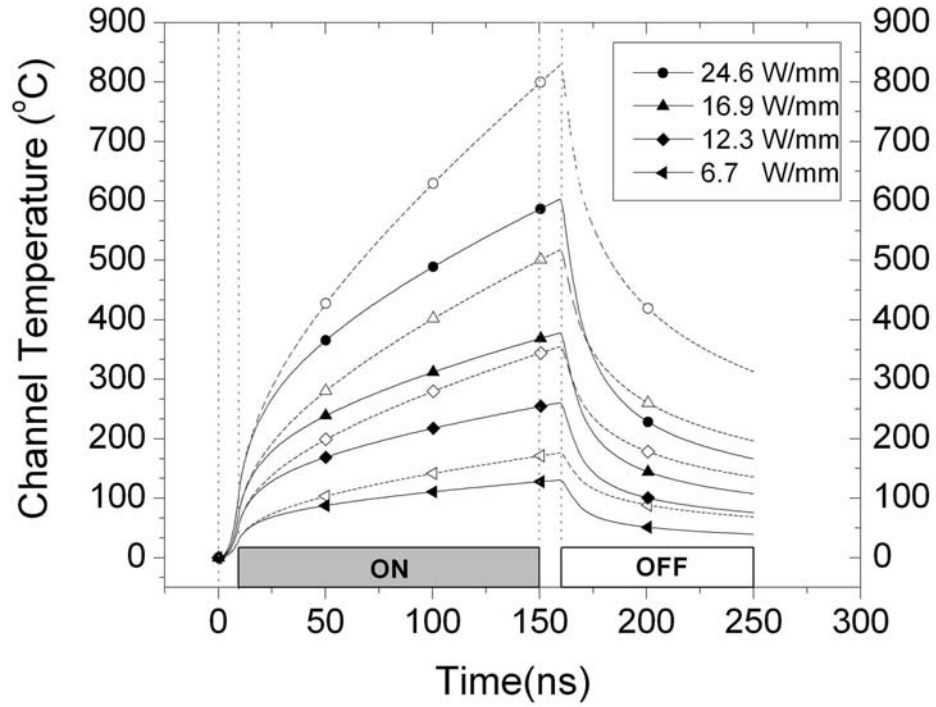


Figure 4.11: Temperature rise in the channel as a function of time and dc power dissipation. The temperature is probed at the center of the 50  $\mu\text{m}$  wide, 125 nm long channel on 25  $\mu\text{m}$  thick SiC (dotted) and 40  $\mu\text{m}$  thick diamond (solid) substrate. Pulse duration is 150 ns with 10 ns rise and fall times.

Thermal boundary resistance at the epilayer-substrate interface, measured by Kuball *et al.* [25] has not been modeled. Peltier/Thomson effects are also ignored. The duty cycle of the pulsed power source is set low enough for the diode to cool down to near the ambient temperature before the rise of the next pulse. This ensures decoupling of the effect of each heat dissipation cycle.

Simulation results presented in Figure 4.12 indicates that 40  $\mu\text{m}$  CVD diamond substrate performs better than back-side thinned 25  $\mu\text{m}$  SiC as a heat sink. Note that the thermal load of the substrate does not show up in the channel temperature up until between 20 ns and 50 ns pulse time. This is understandable since heat energy spread takes a finite amount of time. The oscillator design utilizing the 125 nm long diode

discussed in section IV dissipates 22.5 W/mm dc power at 2.2% efficiency and, the channel temperature rise for this diode is predicted  $\sim 300^\circ\text{C}$  on diamond and  $\sim 350^\circ\text{C}$  on SiC with 50 ns pulsed biasing. Moreover, the same diode can be operated at 12W/mm dc dissipation with 1.8 % efficiency and the temperature rise for this case would be  $\sim 165^\circ\text{C}$  on diamond and  $\sim 200^\circ\text{C}$  on 4H-SiC for the same pulse length (Figure 4.6).

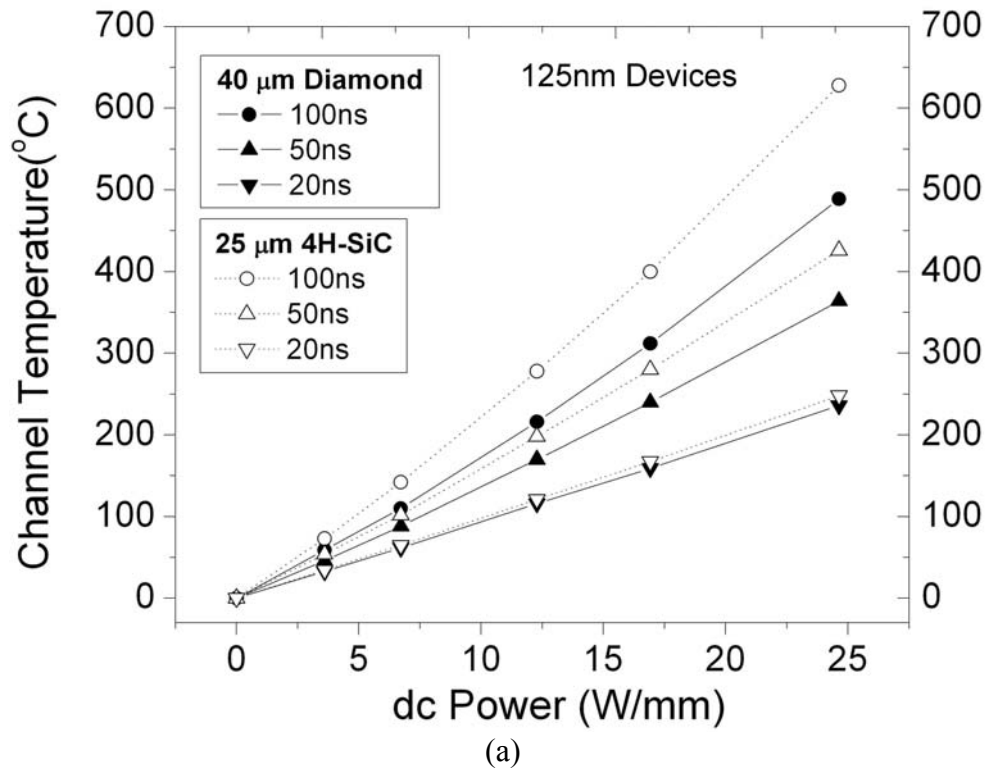
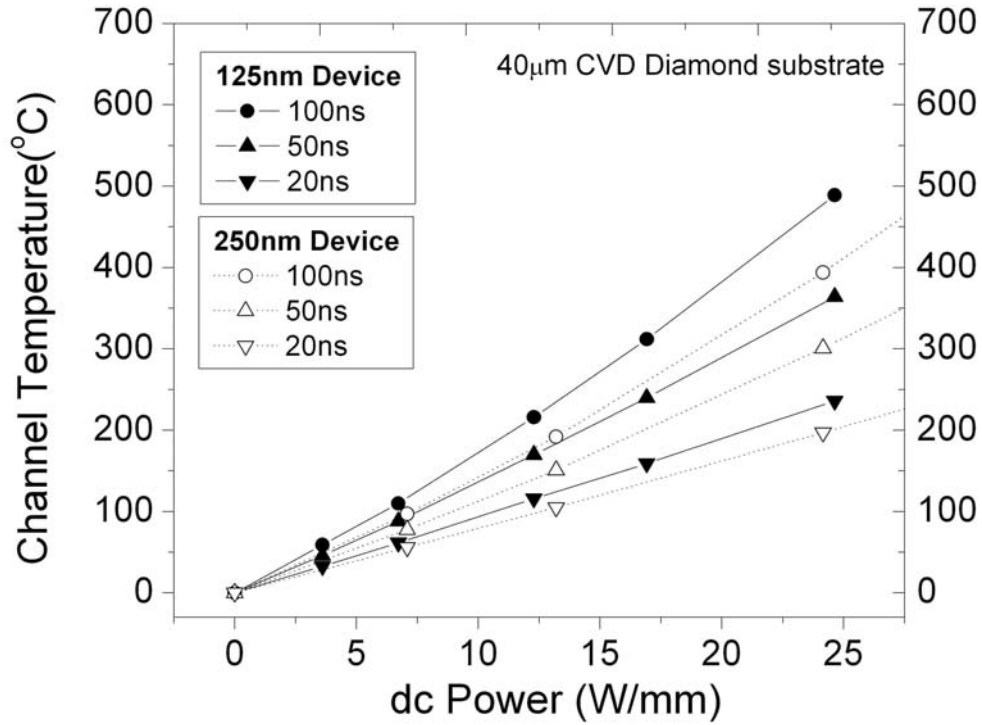


Figure 4.12: Channel temperature rise as a function of dc power dissipation (a) comparing CVD diamond and SiC host substrates. (b) 125 and 250 nm diodes on CVD diamond substrate.

Figure 4.12 continued.

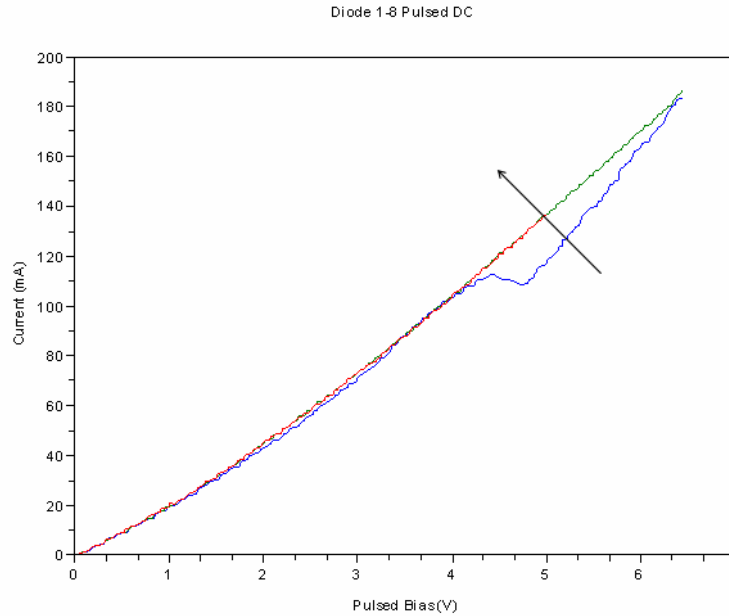


(b)

In the simulations presented above, the power dissipation was assumed to be ohmic. In these ultra-short diodes however, the spatial extent of the hot electron energy relaxation will be longer if we assume the optical phonon emission to be the only energy loss mechanism for the hot electrons. For a ballistically accelerated electron to dissipate 2 eV of kinetic energy for instance, approximately 20 L.O phonon emissions are needed each with 92 meV energy. If we assume a mean free path of ~20 nm, a total of ~400 nm transit distance is necessary to dissipate all kinetic energy. This will lead to a reduction in the power density per square centimeter and thus a cooler operation. See Figure 4.12b to compare the temperature rise in a 125 and 250 nm diodes when dissipating the same amount of dc power.

## 4.8 Experimental Results

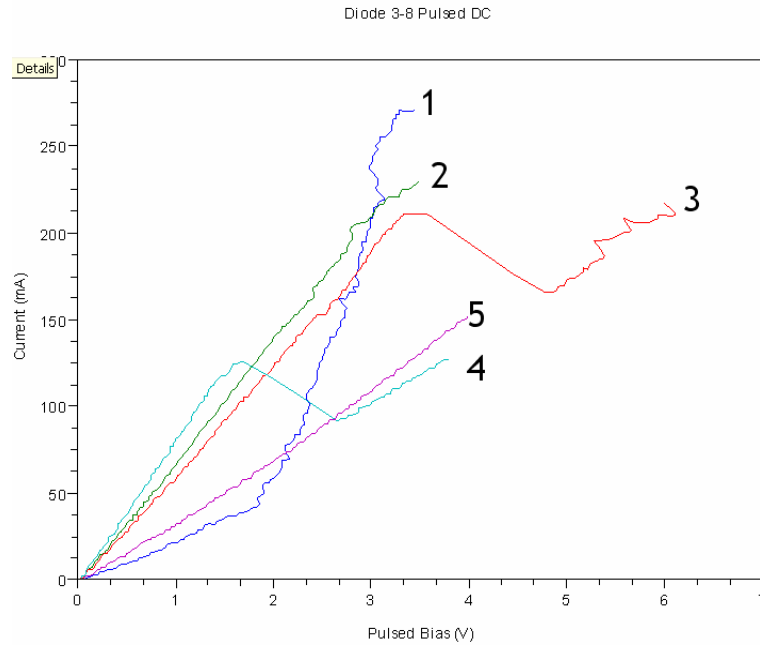
Preliminary experiments did not provide any conclusive data to judge the device concept. Various gap spacings with different diode widths have been fabricated on a 40  $\mu\text{m}$  diamond substrate after much process development [47]. The automated 200 ns long, low-duty-cycle pulsed voltage sweeps (shown in Figure 4.13) indicated significant thermal instability. Despite the fact that the first sweep reveals an NDR like region in the I-V curve, second sweep produces the I-V curve of a pure resistor following the low field resistance of the previous one. This data is not conclusive since the critical etch which has to remove all  $n^{++}$  material was not sufficiently characterized. As suggested by the relatively higher current level, It likely that some  $n^{++}$  layer still remained atop the channel, electrically in parallel, which non-uniformly burns out as the bias is increased. These measurements were performed on the chip shown in as is the case with this chip.



(a)

Figure 4.13: A 25  $\mu\text{m}$  wide horizontal diode with (a) 250 nm gap (b) 130 nm gap [47].

Figure 4.13 continued.



(b)

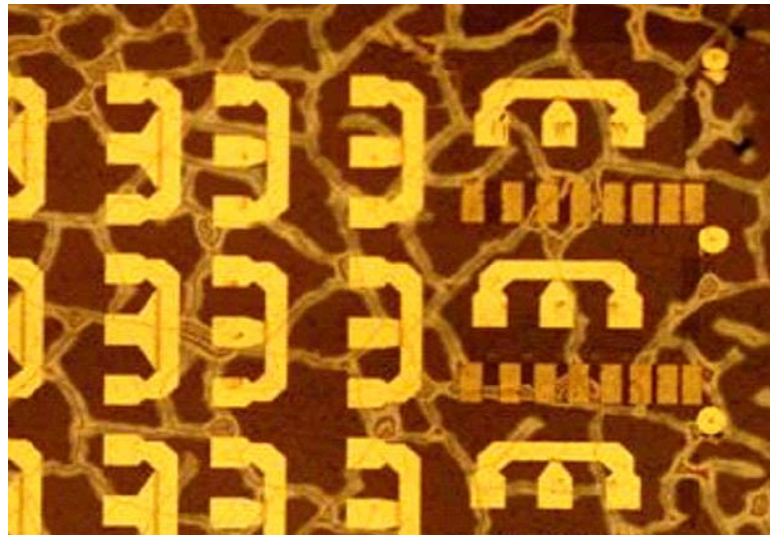


Figure 4.14: Optical microscope photograph of the GaN on (CVD) Diamond chip. Ultra thin epilayers usually delaminate from the diamond substrate and shatter during the fabrication.

## 4.9 Chapter Conclusion

A novel GaN diode exhibiting a strong NDC behavior through the utilization of transient ballistic effects which is capable of generating tens of milliwatts of THz power is proposed and large-signal simulation results along with transient thermal simulations are presented. The field dependence of the electron drift velocity is constructed directly from experimental measurements. Despite the quasi-static and drift-diffusion assumption, key features of the device performance are captured. The coplanar device geometry and relatively higher load resistance requirements of the designs compared to the usual  $50\ \Omega$  condition allows the possibility of radiating vertically outwards through the gap of the channel as shown in Figure 4.15.

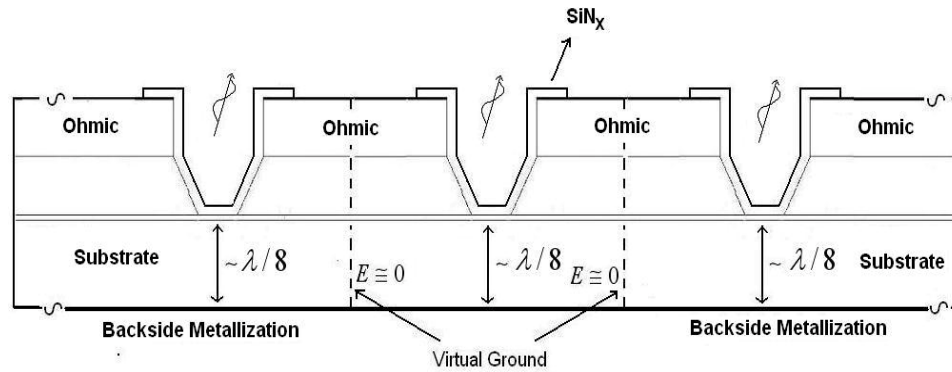


Figure 4.15: Proposed array structure for coherent high power THz radiation. Resonance is with the backside metallization and  $\text{Si}_3\text{N}_4$  slab provides free space matching and passivation of the GaN surface. The design parameters are the diode width and spacing.

$\text{Si}_3\text{N}_4$  can be used to passivate the GaN surface. Through controlled backside etching and metallization of the substrate, one can create the necessary circuit resonance and also improve thermal conduction. An array configuration of these elements, as depicted in

Figure 4.15, would allow high output power and enhance the resonance condition by creating a virtual ground plane between the diodes as a result of the field symmetry.



## CHAPTER 5

# Quasi-ballistic Horizontal NDC Diode Processing

### 5.1 Introduction

The process development for the quasi-ballistic horizontal device revolved around strategies in order to achieve a successful channel definition both in horizontal and vertical directions. This structure is basically an ungated ultra-short MESFET. Horizontally, e-beam lithography sufficed to pattern the necessary gap on Carbon mask to produce 100 – 500 nm spacings for the necessary quasi-ballistic transport. The most challenging aspect of this process was; however, to accomplish the vertical etch such that, following the removal of the 200 nm of  $n^{++}$  GaN, it would be possible to stop precisely on the 20 nm thick channel. Due to  $10^{20} \text{ cm}^{-3}$  doping, even 10 angstroms would introduce enough parallel conductivity to obscure the device operation, and too much penetration into the channel would probably lead to a totally depleted thin layer.

### 5.2 Process Flow

As usual, the process run begins with sample cleaning using solvents in an ultrasonic bath. Next, the alignment marks are put down for accurate overlay. These marks include both e-beam and stepper marks. This step is followed by the device isolation etch. Following another solvent cleaning routine, to ensure the cleanest surface possible, 100 nm amorphous carbon followed by 4 nm of  $\text{SiO}_2$  is deposited in vacuum.  $\text{SiO}_2$  is deposited to pattern carbon. Then, e-beam lithography is put down to define the active diode region ranging from 100 nm – 1  $\mu\text{m}$  channel length. Initially  $\text{SiO}_2$  was

patterned in Plasma Therm 72 tool using  $\text{CF}_4$  for 20 seconds at 30 % RF power and at a pressure of 40 mTorr. The process moves then moves on to the patterning of  $\sim 50$  nm thick carbon in  $\text{O}_2$  plasma. This thickness is required since the particular low etch rate recipe developed has a selectivity of only  $\sim 3:1$  between GaN and carbon. Carbon is patterned in  $\text{O}_2$  plasma in Pt72 (4 min).

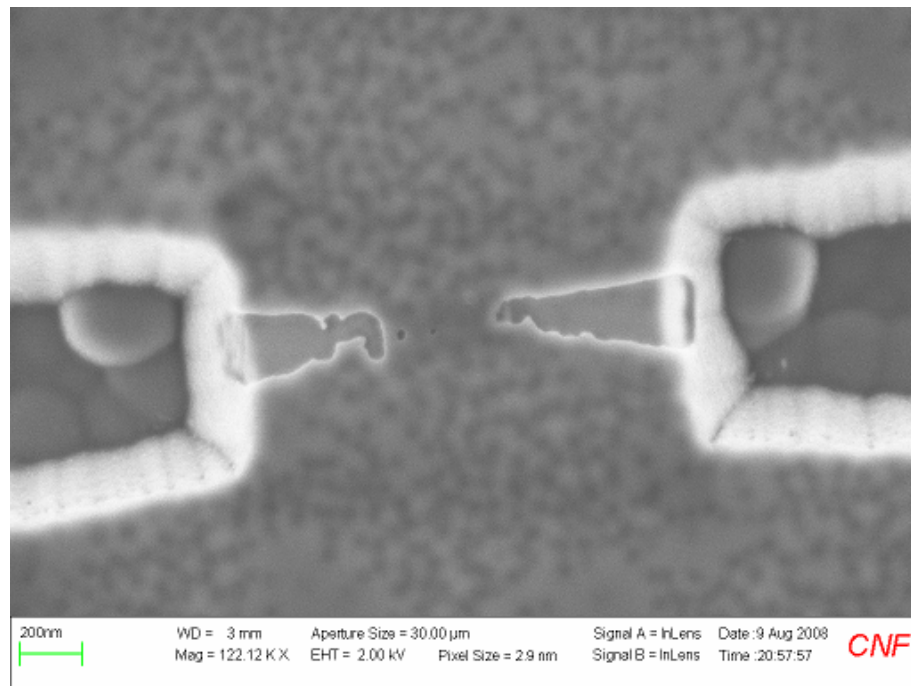


Figure 5.1: SEM image of patterned carbon – on one of the narrow devices. Clearly showing that 20 seconds in  $\text{CF}_4$  did not clear all the  $\text{SiO}_2$  uniformly.

As the SEM characterization revealed (Figure 5.1), the first attempt was unsuccessful. This image was taken after the carbon etch and indicates that the  $\text{SiO}_2$  was not completely removed during  $\text{CF}_4$  etch. This whole lithography process was repeated with 40 seconds  $\text{SiO}_2$  etch in  $\text{CF}_4$  and, the success of this etch was confirmed by SEM characterization after the carbon etch (Figure 5.2).

Before the critical channel etch, the exact carbon mask height and uniformity is carefully mapped using AFM and recorded. This is critical for the accurate book keeping of the etch depths and to successfully stop the etch before punching through the channel.

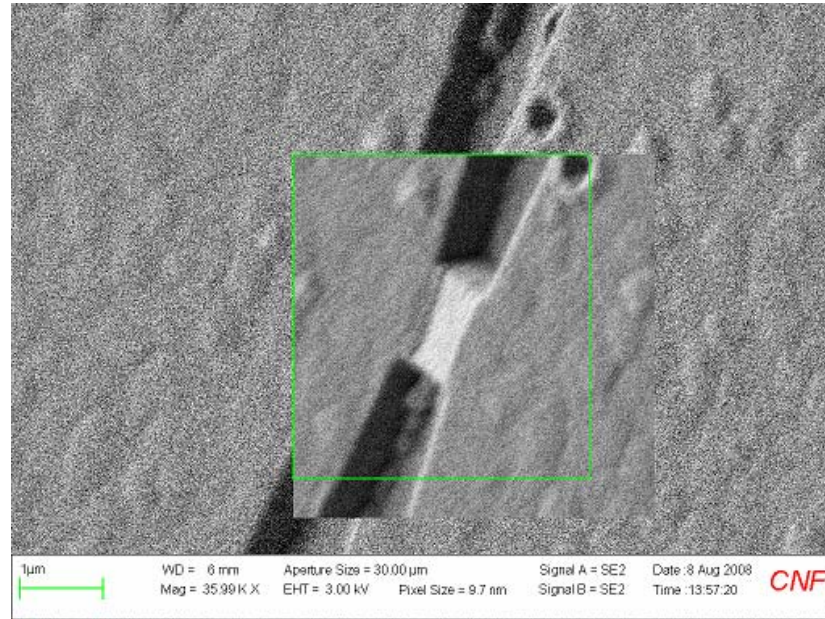


Figure 5.2: SEM image confirming the success of carbon patterning.

ICP etching and AFM characterization followed back and forth about 14 times. There are also other dummy features scattered on the chip purported to increase the accuracy of the bookkeeping. When all calculations and measurements confirm that the desired depth is reached, ICP etch is stopped and the remaining carbon is ashed in  $O_2$  plasma for another 5 minutes. However, in our first attempt AFM characterization of the gaps showed an over etching of 30-45 nm through out the chip. Basically, this meant only 5 nm or nothing was left of the channel. The whole process was repeated by the author 3 times from scratch with a new sample and by Quentin Diduck on GaN on Diamond samples (part time post doctoral researched in our research group at the time) and failed each time. Quentin preferred Ion Milling to ICP and that is what he used

through out. One of the process runs he carried all the way to the end and the results were discussed in the previous chapter.

### 5.3 Summary

Table 5-1: Quasi-ballistic horizontal diode process flow

Step	Parameter
Sample Cleaning	<ul style="list-style-type: none"> <li>▪ Acetone, IPA rinse, N<sub>2</sub> blow dry.</li> <li>▪ DI water rinse, N<sub>2</sub> blow dry</li> <li>▪ 15 °C de-hydration bake on hotplate, 3 minutes.</li> </ul>
Alignment Marks	<ul style="list-style-type: none"> <li>▪ Deposition of ti/pt marks</li> </ul>
Hard Mask Deposition	<ul style="list-style-type: none"> <li>▪ No lithography, Deposit Carbon 0.5 A/s at 1e-7 Torr pressure. Deposit 4 nm Si<sub>2</sub>O to mask and pattern Carbon. 0.5 A/s dep. rate</li> </ul>
Patterning Si <sub>2</sub> O	<ul style="list-style-type: none"> <li>▪ E-beam lithography patterning to define the channel. 100 – 400 nm feature size.</li> </ul>
Si <sub>2</sub> O etch	<ul style="list-style-type: none"> <li>▪ P772 etching. 0.57 minutes of CF<sub>4</sub> etch (40 mTorr, 30 % power)</li> </ul>
Carbon Etch in O <sub>2</sub>	<ul style="list-style-type: none"> <li>▪ Etching the Si<sub>2</sub>O masked Carbon in O<sub>2</sub> plasma. PT72.</li> </ul>
Pre-Etch characterization	<ul style="list-style-type: none"> <li>▪ Pre-Etch mask height and uniformity characterization</li> </ul>
Critical GaN etch	<ul style="list-style-type: none"> <li>▪ Etch GaN.</li> </ul>
Isolation Etch	<ul style="list-style-type: none"> <li>▪ Define the device area using Photolithography. Etch as deep as possible.</li> </ul>
Passivation (Si <sub>3</sub> N <sub>4</sub> dep.)	<ul style="list-style-type: none"> <li>▪ To passivate exposed surface of GaN channel.</li> </ul>
Si <sub>3</sub> N <sub>4</sub> etch	<ul style="list-style-type: none"> <li>▪ This is required for electrical contact to the device</li> </ul>
Ohmic Deposition	<ul style="list-style-type: none"> <li>▪</li> </ul>
Electroplating	<ul style="list-style-type: none"> <li>▪ For better conductivity and heat removal.</li> </ul>

If we could overcome this problem, the fabrication process would have continued as follows: Approximately 40 nm of Si<sub>3</sub>N<sub>4</sub> is deposited to passivate the surface in the GSI PECVD tool. Then, the Si<sub>3</sub>N<sub>4</sub> would be removed from locations where electrical contact is necessary to the n<sup>++</sup> layer by means of dry etching. After this etch, ohmic contacts are deposited and annealing is accomplished in incremental steps to allow enough time for hydrogen out-diffuse from Si<sub>3</sub>N<sub>4</sub>. Electroplating the contacts would be the last step to increase electrical and thermal conductivity.

## CHAPTER 6

### Ohmic Contact Studies

#### 6.1 General Remarks

Extremely low resistance ohmic contacts are imperative in the successful implementation of these proposed BEAN diodes. This is particularly challenging for GaN, as compared to the other well studied III-V compounds (GaAs and InP), because of its large bandgap. Contact resistance is one of the key parameters to mitigate the effects of two undesired conditions. The first one is the excessive joule heating at the anode electrode as a result of the extremely high current density proportional to  $I^2 R_C$ . This causes permanent destruction of the contacts before reaching the desired intrinsic layer bias level. Secondly, non-optimum contact resistance drops most of the total applied bias – this is also enhanced by the electron flooded intrinsic layer (injected from the adjacent  $n^{++}$  layers) which presents only an insignificant series resistance. This prevents the establishment of the required high electric field in the ballistic region required for the device operation. The  $n^{++}$  doping does reduce the contact resistance significantly by creating a much thinner schottky barrier, however; it also contributes to the electron flooding of the intrinsic layer. In the light of these initial observations, we performed a series of experiments comparing different composite metal stacks (with appropriate work functions) on  $n^{++}$  GaN. Initially, excellent ohmic characteristics with a specific contact resistivity as low as  $8 \times 10^{-8} \Omega\text{-cm}^2$  were observed with the *as-deposited* ti/al/mo/au composite (a very popular contact to AlGaN/GaN HEMTs), on  $\sim 1 \times 10^{20} \text{ cm}^{-3}$  GaN and above. Specific contact resistivities

of several as-deposited composite stacks are presented in Figure 6.1. The contact parameters are extracted using standard rectangular TLM methods.

## 6.2 Sample Processing

The epilayers used in these experiments were grown on c-face sapphire substrates using a GEN2 molecular beam epitaxy system. They consisted of an AlN buffer and a  $\sim 1\mu\text{m}$  Germanium doped bulk n-GaN. Three different doping profiles of  $2.93 \times 10^{20} \text{ cm}^{-3}$ ,  $1.26 \times 10^{20} \text{ cm}^{-3}$  and  $4.56 \times 10^{20} \text{ cm}^{-3}$  were used in the experiments. These doping levels were confirmed by Hall measurements.

Following acetone cleaning in ultra-sonic bath to remove particles and dirt, mesas required by the TLM method, are electrically isolated through dry etching all the way down to the substrate using a chlorine based chemistry in an Inductively Coupled Plasma reactive ion etch (ICP-RIE) etch system. Next, rectangular contact pads were patterned on these electrically isolated mesas using bi-layer photolithographic lift-off technique (with incremented gap spacing), and different composites were deposited on different chips. All metal layers except Au were evaporated using e-gun while Au was deposited using thermally, both at a background pressure of  $1.5 \times 10^{-6}$  Torr. Also, within a few minutes prior to deposition, samples were treated with Buffered Oxide Etch (30:1) for 30 seconds to remove the native oxide on the surface. Lift-off was accomplished overnight in (Microchem.) 1165. Next, rapid thermal annealing of the samples were performed in  $\text{N}_2$  ambient.

On-wafer current-voltage measurements were performed at room temperature using Four-point-probe technique to eliminate the effects of resistance between the probes and metal contacts. The real gap spacings were measured under an optical microscope

prior to the I-V measurements and their calculated root-mean square (RMS) values (due to imperfect edge acuity) are used on the abscissa.

The specific contact resistivity, sheet resistance and the transfer length were extracted from a linear curve fit of the measured resistance versus gap spacing plot using the transfer length method (TLM). The correlation coefficient which parameterized the quality of the linear fit were in the 0.9997 – 0.9999 range.

### **6.3 Results and Discussions**

Based on the initial as-deposited measurement results and observations, we used non-alloyed ti/al/mo/au composite as contacts to one of the negative mass vertical diode process runs. However, the voltage seep I-V measurements revealed that the contacts were thermally unstable. Extreme nonuniform self-heating changed the overall contact resistance within the fraction of a second during which the bias was swept. This was deduced from the observation that every successive voltage sweep on the same particular device produced a different and very noisy I-V curve. This suggested that the aluminum with its  $\sim 660^{\circ}\text{C}$  melting point, was locally melting and balling up and thus changing the overall specific contact resistance.

Three other important observations were made from these experiments. Firstly, it was oddly observed that the presence of aluminum in the ti/al/mo/au composite *did* make a difference in comparison to ti/mo/au composite despite both being non-alloyed. Ti was expected to determine the barrier height (0.23 eV) but seems to be that aluminum has to do something with it.

Another interesting observation was that despite the fact that Hafnium (Hf) barrier on GaN was lower than Ti, (3.9-4.1 =- 0.2 eV), TLM experiments showed consistently much better performance with Ti compared to Hf/al/mo/au.

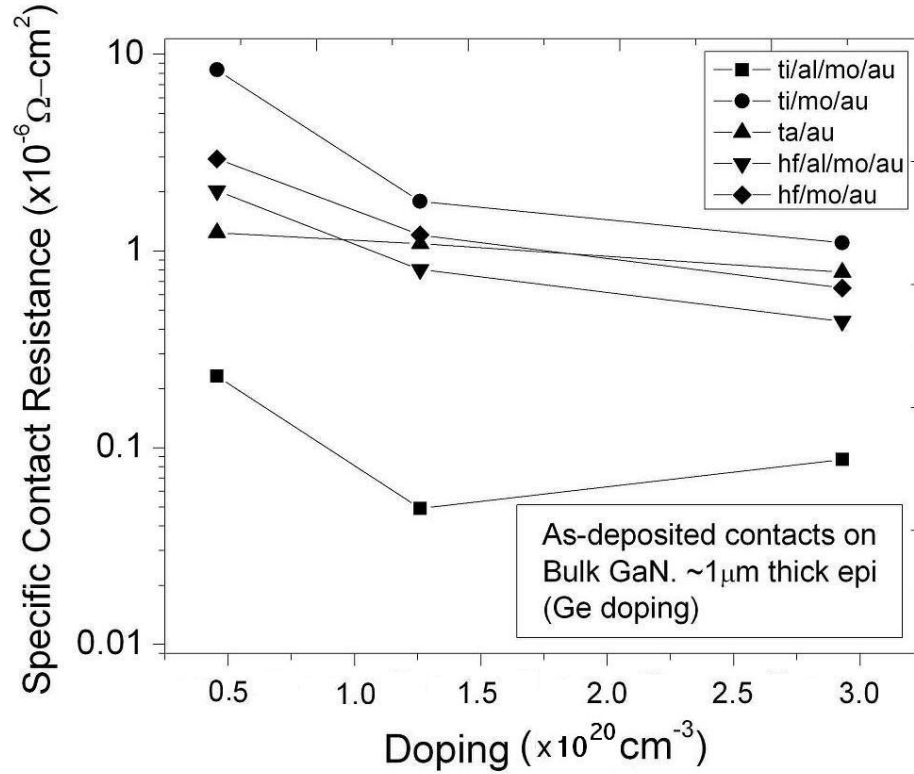


Figure 6.1: As-deposited contacts on bulk GaN. Epilayers were 1  $\mu\text{m}$  thick and Germanium doped.

Having made these observations, we annealed and characterized these experimental samples with TLM patterns all the way up to 800  $^{\circ}\text{C}$  with 50  $^{\circ}\text{C}$  increments. The results are presented in Figure 6.2. The temperature of 550  $^{\circ}\text{C}$  seems to be the second optimum annealing temperature next to ‘as-deposited’. All curves make a dip at that point. One unexpected observation was that annealing even at low temperatures like 350  $^{\circ}\text{C}$  made a significant difference in the specific contact resistance. This suggested that the phenomena had to do with diffusion at low temperatures and itself may be worthy of investigation.



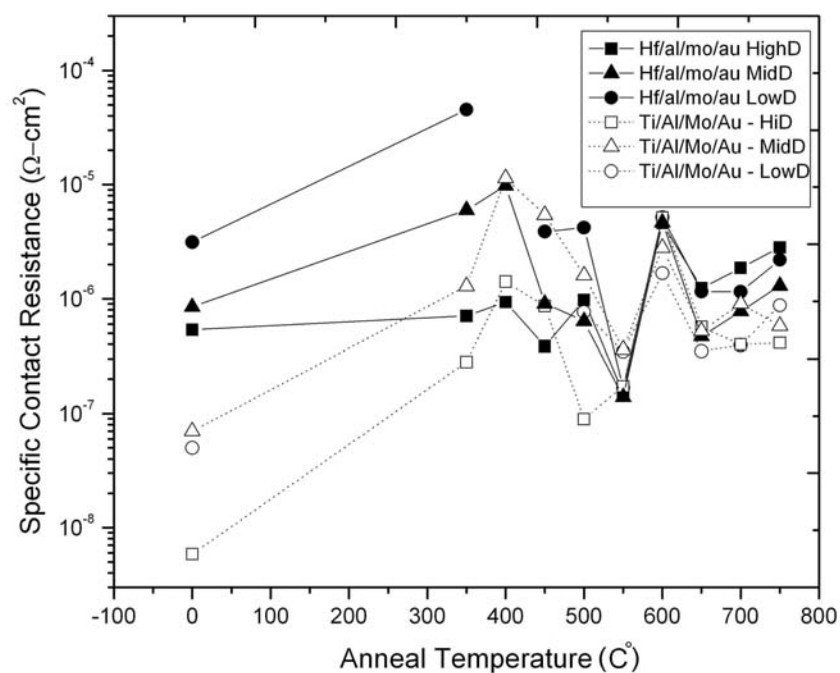


Figure 6.2: Specific contact resistance vs. anneal temperature. Measurements were performed on six samples with different composite metal stacks and doping levels.

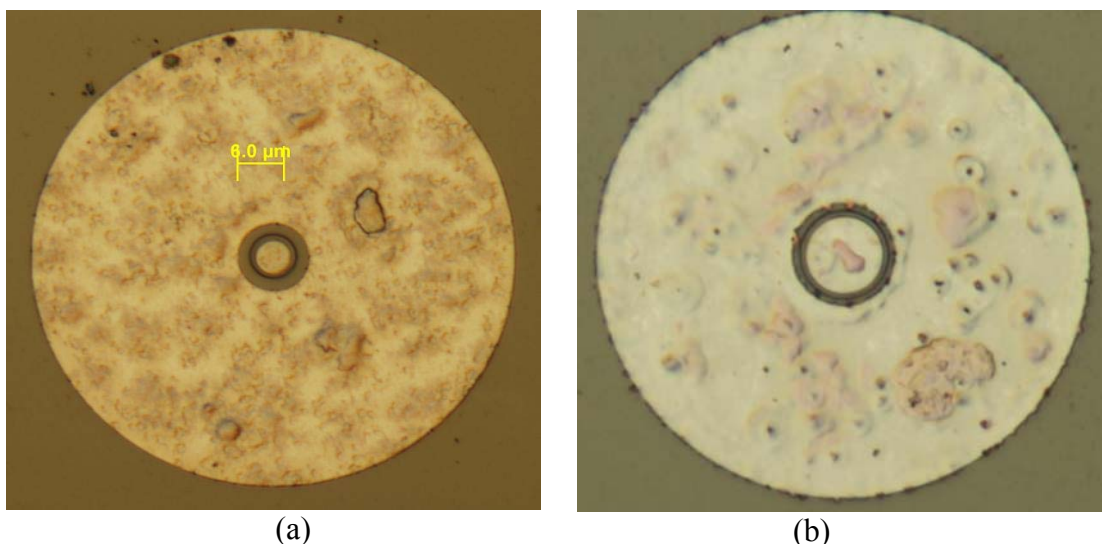


Figure 6.3: Optical microscope photographs comparing surface morphology after (a) 800 °C and (b) 550 °C rapid thermal annealing – showing Aluminum ball up due to melting.

However; from a practical perspective we had to focus on the achievement of the main project objectives and move on with the contact investigations. It should be noted that the RTA is calibrated for emissions from silicon and the temperatures mentioned in this section are not exact because of this. A better way would be to construct a silicon housing made from pieces around the GaN sample to simulate the effect, however; this was not crucial and omitted. In Figure 6.4, sheet resistance measured on different samples is plotted against its doping. The diminishing nature of the benefit is clearly visible from this data beyond roughly  $1 \times 10^{20} \text{ cm}^{-3}$  doping. This can be attributed to decrease in mobility whose effect is compensating and surpassing the effect of increased carrier density.

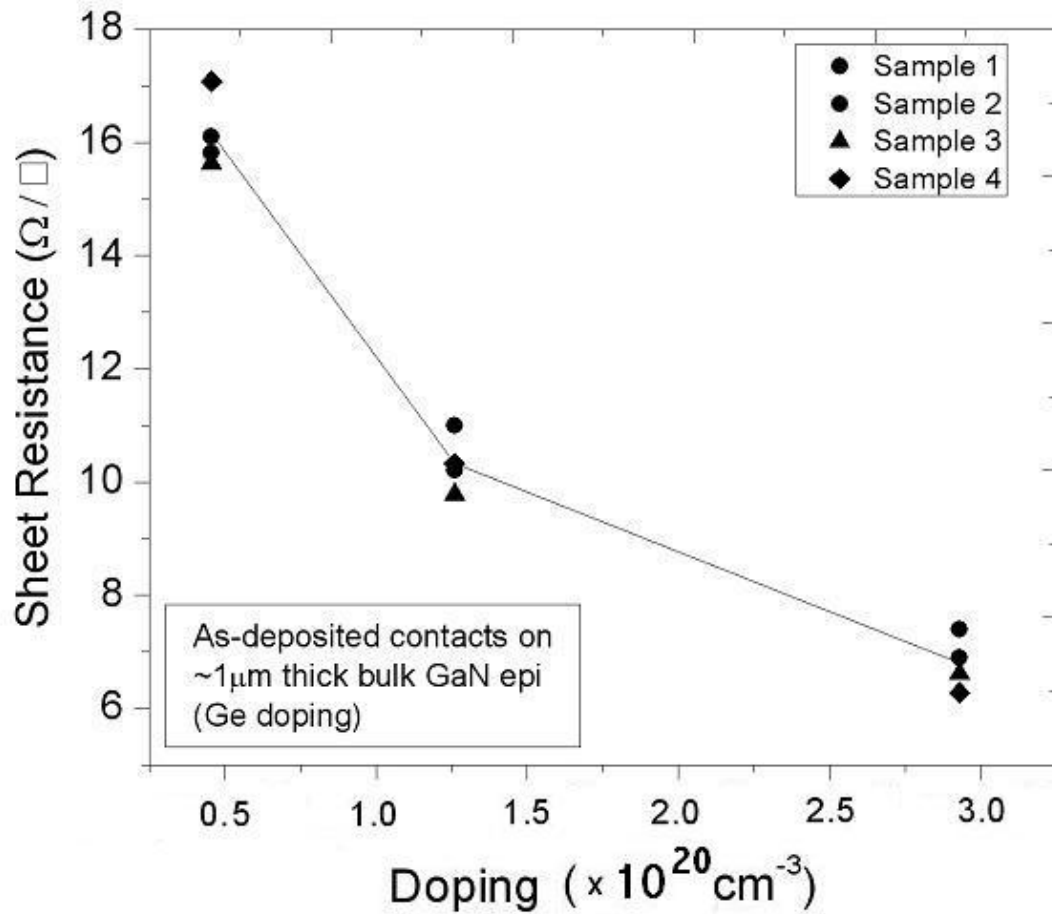


Figure 6.4: Sheet resistance vs. doping. GaN epilayers thicknesses on all four samples were  $\sim 1 \mu\text{m}$ .

In the light of these experiments, it has been shown that ti/al/mo/au annealed at 800 °C is still a great ohmic contact to  $n^{++}$  doped GaN just like it is to AlGaIn/GaN HEMTs. As-deposited usage of this composite may be valuable for low power applications but certainly not for the BEAN diode where such high dc power dissipation and consequent temperature rise have to be endured. The temperature of 800 °C RTA annealing condition proved to be a viable route to create thermally stable, low resistance ohmic contacts on highly doped n-type GaN.

## CHAPTER 7

### Summary and Conclusions

The main effort in this PhD research was directed towards implementing Ridley et al's negative effective mass diode concept based on ballistic electron acceleration (see CHAPTER 2) in GaN epilayers in order to harness its fast NDC property in a resonant circuit to generate THz power. It is a two terminal diode with a channel length in the order of an electron mean free path ( $\sim 20 - 30$  nm). An electric field of 1 MV/cm strength is necessary in this channel to accelerate the majority the electrons ballistically beyond the inflection point in the conduction band into the negative effective mass states. This slows them down when the field is further increased and thus leads to a negative differential conductivity. According to the theory, the electrons need to be injected with finite energy in order to overcome certain transit time related complications which would otherwise prevent NDC.

Despite the achievement of important mile stones towards this goal, two main technical obstacles prevented the experimental demonstration of the phenomena: (i) The tremendous thermal energy resulting from more than 1 MA/cm<sup>2</sup> current density through the top electrode with typical ohmic contact resistivities ( $> 1 \times 10^{-6} \Omega\text{-cm}^2$ ). (ii) Biasing the active region with 1 MV/cm electric field --  $\sim 30$ nm intrinsic layer inserted between  $10^{20} \text{ cm}^{-3}$  doped  $n^{++}$  layers before the device is permanently destroyed by the above mentioned joule heating. As a result, during the course of this research, this device concept had been temporarily shelved in order to pursue a seemingly more feasible device geometry based on quasi-ballistic effects (drawn from Wraback et al's experiments). However, in retrospect, the author is convinced that the

negative effective mass wall-type diode structure, which was presented at the end of Chapter 2, is the has the most potential towards realizing this revolutionary device idea.

The quasi-ballistic diode approach is also very promising. Assuming one can construct a velocity-field characteristic curve from transient velocity-time measurements of a laser induced accumulation layer of electrons, we have predicted, through simulations, excellent device performance as part of a resonant circuit designed for THz oscillations [48]. In addition, thermodynamic simulations of the device under the designated bias conditions have also been performed and predict feasible operating channel temperatures (see CHAPTER 4 for details). This device resembles an ungated MESFET structure with a 20 nm thick  $1 \times 10^{18} \text{ cm}^{-3}$  doped channels (Figure 4.3).

Despite the exciting theoretical predictions, again the decisive experimental verification of these results has not been achieved due to major processing challenges and uncertainties. The greatest challenge was to etch and keep precise track of a thick (50 nm– 200 nm)  $n^{++}$  GaN and stop dead on the 20-40 nm thick channel epilayer without punching through it. A significant depletion of this channel was also expected due to its small thickness raising more uncertainty in the interpretation of the results and preparing a new action plan. To fully exploit the potential of this idea, a feasible and reproducible fabrication technique is still to be developed.

# APPENDIX

## A. Silvaco Codes

### A.1 Electrodynamic Simulation Code

```
go atlas
mesh
# ***** ASSIGNING VARIABLES *****
set FILE=S15D250_#1Exp601
set Bias=12
set RLoad=500
set Bindu=3.30e-12
set Cdev=3.45e-15
set SimDt=1e-14
set MyDtMin=3.5e-15
set ftime=30e-12
set length=0.25
set Res=0.003
set DevWidth=333.3
set LatMesh=0.003
set ChanDoping=1E+18
set NPlusDoping=1E+20
set Nplus=0.01
set PerStr=20
set Location=0.3
set Reduction=4
set ext=.str
set ext2=_inst
set ext3=_tr.log
set extdatVD=_DEVIVoltage.dat
set extdatIL=_LOADCurrent.dat
set extdatID=_DEVICurrent.dat
set stime=0.01e-12
set      w=$LatMesh

set p_vsatn      = 2.0e+7
set p_mun        = 260

# ***** CREATING THE STRUCTURE *****
y.mesh loc=(-$length/2)-$Nplus      spac=$Res
y.mesh loc=(-$length/2)             spac=$Res/$Reduction
y.mesh loc=(-$length*$Location)     spac=$Res
y.mesh loc=($length/2)-0.005        spac=$Res
y.mesh loc=($length/2)              spac=$Res/5
y.mesh loc=($length/2)+$Nplus       spac=$Res/5

x.mesh loc= -$w/2 spac=$LatMesh
x.mesh loc=  $w/2 spac=$LatMesh

region num=1 x.min=-$w/2 x.max= $w/2 y.min=(-$length/2)-$Nplus
y.max=($length/2)+$Nplus material=GaN
elec num=1 name=anode x.min=-$w/2 x.max= $w/2 y.min=(-$length/2)-$Nplus
y.max=(-$length/2)-$Nplus
elec num=2 name=cath1 x.min=-$w/2 x.max= $w/2 y.min=($length/2)+$Nplus
y.max=($length/2)+$Nplus
```

```

doping
uniform conc=$ChanDoping n.type
doping x.min=-$w/2 x.max= $w/2 y.min=(-$length/2)-$Nplus y.max= -$length/2
uniform conc=($NplusDoping-$ChanDoping) n.type
doping x.min=-$w/2 x.max= $w/2 y.min=$length/2
y.max=($length/2)+$Nplus uniform conc=($NplusDoping-$ChanDoping) n.type
save outfile=$FILE'.str'

#_____

go atlas
.BEGIN
VS 2 0 0 pulse 0 $Bias 0 2ps 2ps 150ps 1000ps
LL 2 1 $Bindu
C1 1 0 $Cdev
RL 1 0 $RLoad

AGUNN 0=cath1 1=anode WIDTH=$DevWidth INFILE=$FILE$ext
.NODESET V(1)=0 V(2)=0
.NUMERIC LTE=1e-7 TOLTR=5.0E-5 dtmin=$MyDtMin VCHANGE=10
.OPTIONS PRINT WRITE=$PerStr*4
.LOG OUTFILE=$FILE
.SAVE MASTER=$FILE$ext2
.TRAN $SimDt $ftime
.END

material DEVICE=AGUNN material=GaN permittivity=9.7 f.munsat=gansat250.lib
mobility DEVICE=AGUNN mun=$p_mun vsatn=$p_vsatn

models DEVICE=AGUNN print temperature=300 fldmob
output e.mob e.velocity j.disp j.diff

method carriers=1 electron maxtraps=10 \
      tol.relax=1 autonr dvmax=100

probe DEVICE=AGUNN name="n0" x=0 y=(-$length/2)+0.0150 n.conc
probe DEVICE=AGUNN name="n1" x=0 y=(-$length/2)+0.0151 n.conc
probe DEVICE=AGUNN name="n2" x=0 y=(-$length/2)+0.0175 n.conc

probe DEVICE=AGUNN name="Vel" x=0 y=(-$length/2)+0.015 vel.electron
dir=90
probe DEVICE=AGUNN name="E" x=0 y=(-$length/2)+0.015 field dir=90
probe DEVICE=AGUNN name="JDiff" x=0 y=(-$length/2)+0.015 j.disp dir=90
probe DEVICE=AGUNN name="JDisp" x=0 y=(-$length/2)+0.015 j.diffusion
dir=90
probe DEVICE=AGUNN name="JCond" x=0 y=(-$length/2)+0.015 j.conduction
dir=90
probe DEVICE=AGUNN name="JTotal" x=0 y=(-$length/2)+0.015 j.total dir=90
probe DEVICE=AGUNN name="Jelect" x=0 y=(-$length/2)+0.015 j.electron dir=90
probe DEVICE=AGUNN name="Mobility" x=0 y=(-$length/2)+0.015 n.mob dir=90

go atlas
extract init inf="$FILE$ext3"
extract name="VD" curve(time, vcct.node."V[1]" ,x.min=$stime
x.max=$ftime ) outfile="$FILE$extdatVD"
extract name="IL" curve(time, icct.node."RL" ,x.min=$stime
x.max=$ftime ) outfile="$FILE$extdatIL"
extract name="ID" curve(time, icct.node."AGUNN_anode" ,x.min=$stime
x.max=$ftime ) outfile="$FILE$extdatID"
quit

```

## A.2 Thermodynamic Code – under pulsed biasing conditions

```
# ***** EXPLANATIONS *****
# The rise and fall times are 10ns.
# 3rd region is the Channel.
# Device is 50um wide.
# Therm Contact is zero celcius (273K)
# ***** EXPLANATIONS *****

go atlas

set FILE=PT_125nm_25umSiC_273K_3V

set STRFile=PT_125nm_25umSiC.str

set GaNtThFile=ganthermcond.lib

set SUBSThFile=sicthermcond.lib

set Bias=3
set ChanMob=200

set SubsLoc=26
set DevWidth=50
set BackTemp=273

set Rise=10ns
set Fall=10ns
set PulseDr=150ns

set SimDt=20e-11
set MyDtMin=1.5e-11
set ftime=250e-9

set RLoad=220
set Bindu=0.61e-12
set Cdev=4.22e-15
set ext=.str
set ext2=_inst
set ext3=_tr.log

# -----
.BEGIN

VS  2 0 0 pulse 0 $Bias 0 $Rise $Fall $PulseDr 5000ns
LL  2 1 $Bindu
C1  1 0 $Cdev
RL  1 0 $RLoad

AGUNN 0=cath1 1=anode WIDTH=$DevWidth INFILE=$STRFile
```



```

.NODESET V(1)=0 V(2)=0
.NUMERIC LTE=1e-7 TOLTR=1.E-6 dtmin=$MyDtMin VCHANGE=10
.OPTIONS WRITE=50

.LOG OUTFILE=$FILE
.SAVE MASTER=$FILE$ext2
.TRAN $SimDt $ftime
.END

thermcontact DEVICE=AGUNN num=1 f.contemp=contemp.lib x.min=-0.362
x.max=0.362 y.min=$SubsLoc y.max=$SubsLoc
material DEVICE=AGUNN material=GaN permittivity=9.7
f.tcond=$GaNtThFile
material DEVICE=AGUNN region=6 f.tcond=$SUBSThFile

mobility DEVICE=AGUNN region=1 mun=95 tmun=0 tmup=0
mobility DEVICE=AGUNN region=2 mun=95 tmun=0 tmup=0
mobility DEVICE=AGUNN region=3 mun=$ChanMob tmun=0 tmup=0
mobility DEVICE=AGUNN region=4 mun=5 tmun=0 tmup=0

models DEVICE=AGUNN print temp=$BackTemp l.temper

probe DEVICE=AGUNN name="ChnTemp" x=0 y=0 lat.temp
probe DEVICE=AGUNN name="InterfaceTemp" x=0 y=1 lat.temp

go atlas

```

## B. Hard mask characterizations on GaN

The problem of catastrophic failure of the diode contacts, and later, upon confirming this extreme joule heating through the thermal simulations, pushed us to employ hard masks in our process to be able to implement the wall type devices which required high aspect ratio ultra-narrow mesa structures.

The first of these efforts were focused on using thermally evaporated Nickel. Nickel is commonly accepted as a good hard mask on GaN but details of the processes that other groups have developed are quite obscure. In our first trials, following the deposition of the composite ohmic contact metal layers, 100-200 nm nickel was thermally evaporated atop this stack without breaking the vacuum. However; these attempts failed due to a persistent problem and we repeated the process many times with different conditions until it was isolated. The problem was that after the dry etch,

both optical microscope and SEM characterization of the chip revealed (Figure B.1) that the metal layers were severely damaged and relatively large particles of unidentified nature were found on the surface, randomly scattered but more dense around the mesa edges. Because of these particles, it was not possible to profile the mesas in order to measure the metal height, or differentiate the top most layer.

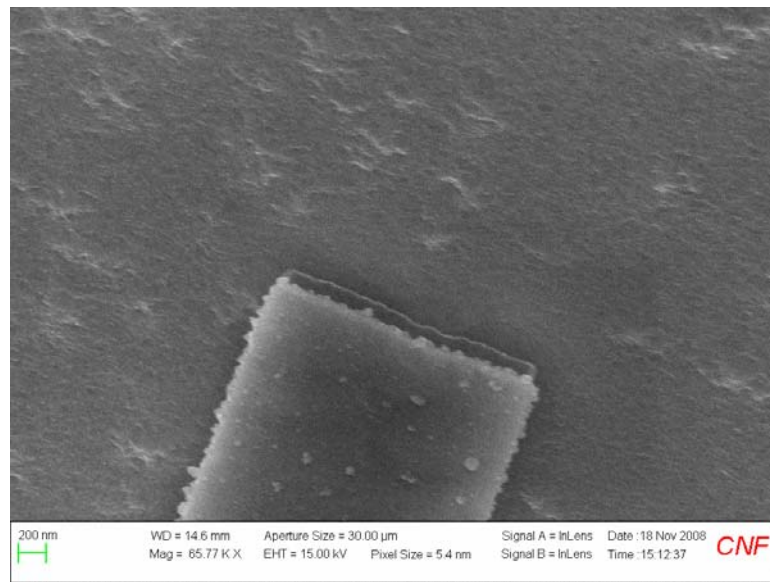


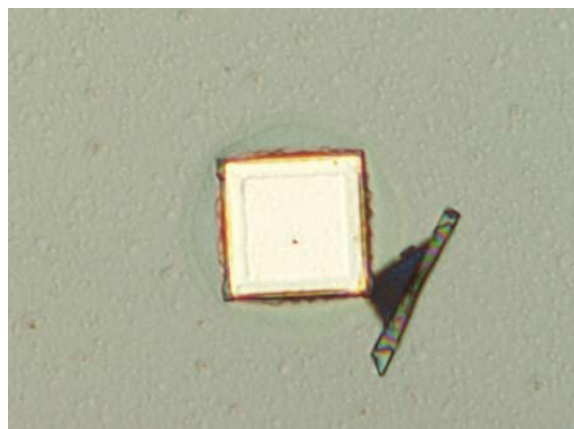
Figure B.1: SEM image showing Aluminum salt formations after punching through the self-aligned nickel mask.

Later on, it turned out that the nickel etch rate using that particular ICP recipe, which relied more on physical bombardment with its 50 Volts sheath bias and 400 Watts ICP power, was much higher than we expected. As a result, before the mesa etch was complete, all the nickel mask was consumed, underlying gold was rapidly sputtered, 45 nm of Molybdenum (Mo) was punched through and Aluminum partially penetrated produced certain aluminum salts due to its reactions with the eth chemistry. After this diagnosis, the problem was solved by developing more suitable recipes through a series of experiments which relied on careful measurement of the Nickel and GaN etch

rates on dummy samples patterned by photolithography. However, there still was an adhesion problem associated with the self-aligned mesa and ohmic metals even after the new etching practice. Figure B.2 shows some mesa features on the same chip illustrating this peeling problem.



(a)



(b)

Figure B.2: Optical microscope image showing metal traces peeled-off (position marks) associated with the nickel protected self-aligned mesa etching.

After giving up on nickel, we began to investigate evaporated amorphous carbon as a hard mask for the wall-type devices. The preliminary experiments using the carbon lithography recipes found in the literature and discussed with the CNF community yielded very promising results. It is difficult to deposit a smooth high quality layer of carbon. However, if the carbon mask is successfully put down and patterned, etching by using it as a mask is relatively easier and predictable. In Figure B.3, the collective results of etch rate and selectivity experiments are presented.

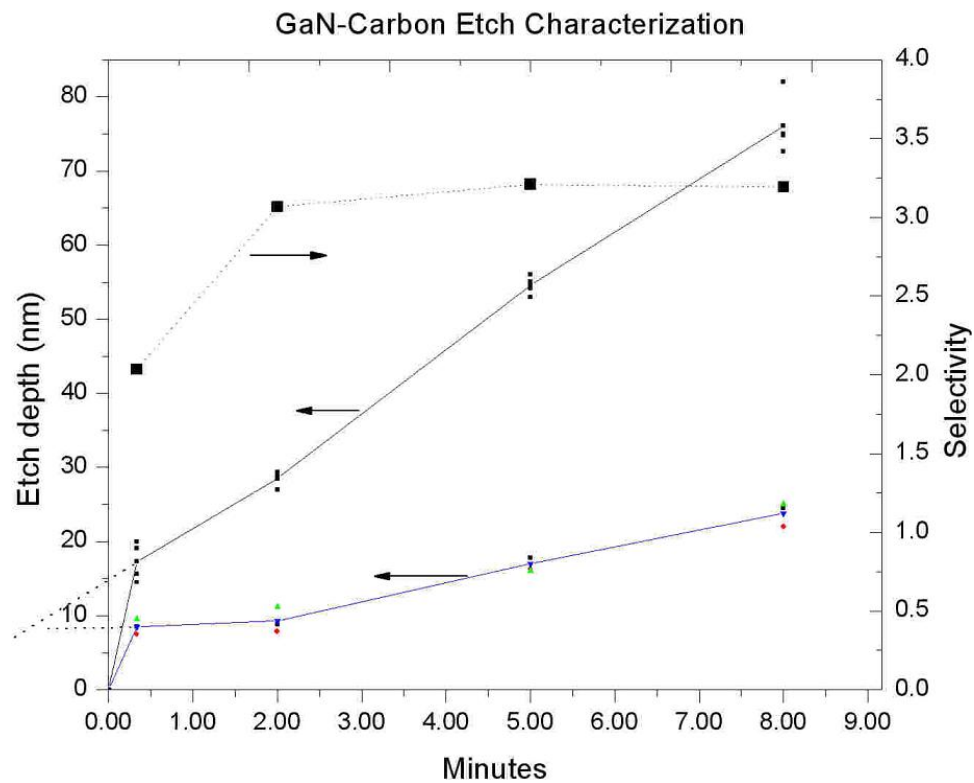


Figure B.3: GaN/Amorphous carbon etch-rate data using recipe 3 in Table B.1. The nonlinearity of etch rate with respect to time is clearly seen for durations less than ~1 minute.

Data shown in Figure B.3 were obtained as a result of our efforts to develop an ultra-controllable low-etch-rate ICP process (for the horizontal diode) that would allow us

to etch ~200 nm of  $n^{++}$  GaN and stop right on the ~20 nm thick GaN channel before punching through it.

Table B.1: ICP etch recipes contrasted for etch rates and GaN-Carbon selectivity

Chemistry	Recipe1	Recipe2	Recipe3
BCL3 (sccm)	17	17	12
Ar (sccm)	8	6	8
Cl2 (sccm)	2	8	0
Pressure (mTorr)	5	6	6
RF1 (W)	35	35	30
RF2 (W)	300	350	100
DC Reading	105	97	53
GaN Rate (nm/min)	30	104	14.8
C Rate (nm/min)	11	15	4

However, it was learned from these experiments that the price of cutting  $Cl_2$  completely and reducing ICP power by a factor of 75 % meant loosing GaN to Carbon selectivity. The role of  $Cl_2$  in etching GaN was obviously chemical (compare recipe 2 and 3 in Table B.1). In a chemistry without chlorine present and very low plasma density, the selectivity between the two materials is solely determined by the physical component of the process.

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